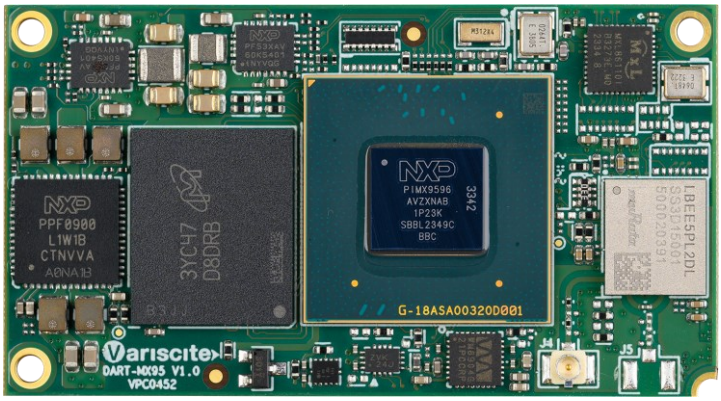
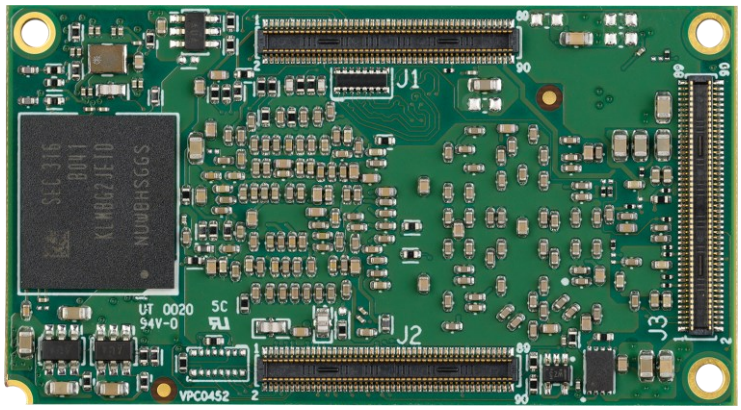
VARISCITE LTD.

DART-MX95 V1.x Datasheet

NXP i.MX 95™ - based System-on-Module





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DART-MX95 Datasheet

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1. Document Revision History

Revision	Date	Notes
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1.01	Aug 8, 2024	Updated Bluetooth version to 5.4
1.02	Aug 14, 2024	Updated section 9.3,11.2 Corrected J1.60, J1.62 ball numbers Corrected typo Alt2 pin J2.34 Updated notes pins J2.02, J2.04, J1.72, J2.11, J2.13, J2.90
1.03	Jan 7, 2025	Corrected section 9.3 units typo Updated pinout according to SOM Rev 1.1 – swapped pins J3.48, J3.50
1.04	Aug 03, 2025	Updated note for pin J1.31

2. Table of Contents

1. Document Revision History 3
2. Table of Contents 4
3. List of Tables 6
4. Overview 8
4.1 General Information 8
4.2 Feature Summary 9
4.3 Block Diagram 10
5. Main Hardware Components 11
5.1 NXP i.MX 95 11
5.2 Memory 16
5.3 Audio (WM8904) 16
5.4 Wi-Fi + BT + LR-WPAN 17
5.5 PMIC 18
5.6 10/100/1000 Mbps Ethernet Transceiver 18
5.7 EEPROM 18
6. DART-MX95 Hardware Configuration 19
7. External Connectors 20
7.1 Board to Board Connector 20
7.2 Wi-Fi & BT Connector 20
7.3 DART-MX95 Connector Pin-out 20
7.4 DART-MX95 Pin-Mux 32
8. SOM's interfaces 39
8.1 Display Interfaces 40
8.2 Camera Interface 43
8.3 Ethernet Interface 45
8.4 Wi-Fi, BT, 802.15.4 52
8.5 MMC/SD/SDIO 57
8.6 USB Ports 58
8.7 PCIe 61
8.8 Audio 63
8.9 LPUART - Low Power Universal Asynchronous Receiver/Transmitter 71
8.10 LPSPI - Low Power Serial Peripheral Interface 76
8.11 FlexSPI - Flexible Serial Peripheral Interface 80
8.12 LPI2C - Low Power Inter-Integrated Circuit 82
8.13 I3C 85
8.14 FlexCAN - Flexible Data Rate CAN 87
8.15 Timer/PWM Module (TPM) 90
8.16 Low-Power Timer (LPTMR) 93
8.17 Flexible I/O (FLEXIO) 94
8.18 ADC 98
8.19 Reference Clocks 99
8.20 GPIO - General Purpose Input Output 100
8.21 DAP - Debug Access Port 106
8.22 Power 107
8.23 System Control 111
9. Electrical specifications 114

9.1 Absolute maximum ratings 114
9.2 Operating conditions 114
9.3 Power consumption 114
9.4 Peripheral Voltage Levels 115

10. Environmental Specifications 116

11. Mechanical Drawings 117

11.1 Carrier Board Mounting 117
11.2 Standoffs 117
11.3 SOM Dimensions 118

12. Legal Notice 119

13. Warranty Terms 120

14. Contact Information 121

3. List of Tables

Table 1: Partial Hardware Configuration Options 19
Table 2: PIN-OUT Tables Mnemonics 20
Table 3: J1 PIN-OUT 21
Table 4: J3 PIN-OUT 28
Table 5: DART-MX95_J1 PINMUX 32
Table 6: DART-MX95_J2 PINMUX 34
Table 7: DART-MX95_J3 PINMUX 38
Table 8: Interface Tables Mnemonics 39
Table 9: SOM Signal Group Traces Impedance 39
Table 10: LVDS0 Signals 40
Table 11: LVDS1 Signals 41
Table 12: MIPI DSI/CSI Signals 42
Table 13: MIPI-CSI2 P0 Signals 44
Table 14: Gigabit Ethernet Magnetics 45
Table 15: Ethernet PHY Signals 46
Table 16: MxL86110x Ethernet PHY LED Behavior 46
Table 17: ENET1 Signals 46
Table 18: ENET2 Signals 49
Table 19: MDIO, Power, 1588, Control & Clock Signals 50
Table 20: 10Gb Signals 51
Table 21: BT LPUART interface signals 54
Table 22: BT PCM interface signals 54
Table 23: WBE SPI interface signals 55
Table 24: WLAN/BT Host Wake 55
Table 25: WIFI control interface signals 56
Table 26: uSDHC2 interface signals 57
Table 27: uSDHC3 Signals 57
Table 28: USB3.0 Port 1 Interface signals 60
Table 29: USB2.0 Port 2 Interface signals 60
Table 30: USB Port 1 & 2 Interface signals 60
Table 31: PCIE1 Signals 61
Table 32: PCIE1 Side band signals 62
Table 33: PCIE2 Signals 62
Table 34: PCIE2 Side band signals 62
Table 35: Analog Audio Signals 63
Table 36: SAI interface signals definition 65
Table 37: SAI1 Signals 65
Table 38: SAI2 Signals 66
Table 39: SAI3 Signals 67
Table 40: SAI4 Signals 67
Table 41: SAI5 Signals 68
Table 42: PDM Signals 69
Table 43: SPDIF Signals 69
Table 44: MQS1 Signals 70
Table 45: MQS2 Signals 70
Table 46: AUD Signals 70
Table 47: LPUART I/O Signals 72
Table 48: LPUART1 Signals 72
Table 49: LPUART2 Signals 72
Table 50: LPUART3 Signals 73
Table 51: LPUART4 Signals 73
Table 52: LPUART5 Signals 74
Table 53: LPUART6 Signals 75
Table 54: LPUART7 Signals 75
Table 55: LPUART8 Signals 75
Table 56: LPSPI1 Signals 76
Table 57: LPSPI2 Signals 78
Table 58: LPSPI3 Signals 78
Table 59: LPSPI4 Signals 78
Table 60: LPSPI5 Signals 78
Table 61: LPSPI6 Signals 79
Table 62: LPSPI7 Signals 79
Table 63: LPSPI8 Signals 79
Table 64: FlexSPI Signals 81
Table 65: LPI2C2 Signals 83
Table 66: LPI2C3 Signals 83
Table 67: LPI2C4 Signals 83
Table 68: LPI2C5 Signals 84
Table 69: LPI2C6 Signals 84
Table 70: LPI2C7 Signals 84
Table 71:LPI2C8 Signals 84

Table 72: I3C Signals 86
Table 73:FlexCAN1 Signals 88
Table 74: FlexCAN2 Signals 88
Table 75: FlexCAN3 Signals 89
Table 76: FlexCAN4 Signals 89
Table 77: FlexCAN5 Signals 89
Table 78: TPM1 Signals 90
Table 79: TPM2 Signals 91
Table 80: TPM3 Signals 91
Table 81: TPM4 Signals 91
Table 82: TPM5 Signals 92
Table 83: TPM6 Signals 92
Table 84: LPTMR1 Signals 93
Table 85: TPM2 Signals 93
Table 86: FLEXIO1 Signals 95
Table 87: FLEXIO2 Signals 96
Table 88: ADC Signals 98
Table 89: Clock Signals 99
Table 90: GPIO Signals 100
Table 91: DAP Signals 106
Table 92: Power Pins 107
Table 93: Ground Pins 108
Table 94: NC Pins 109
Table 95: System Control Signals 111
Table 96: BOOT_MODE Signals 112
Table 97: Available boot sources 113
Table 98: Absolute Maximum Ratings 114
Table 99: Operating Ranges 114
Table 100: DART-MX95 Power Consumption 114
Table 101: Environmental Specifications 116

4. Overview

4.1 General Information

The DART-MX95 offers advanced graphics and video cores, powerful vision and machine learning acceleration, efficient CPU performance plus real-time processing and advanced security with integrated EdgeLock® secure enclave to support energy-efficient edge computing. A rich set of peripherals and processor cores support these features.

The product is based on the NXP i.MX 95 applications processors which integrate up to six Arm Cortex®-A55 cores and are the first i.MX devices to support functional safety with built-in Arm Cortex®-M33 which can be configured as a safety island. Optimizing performance and power efficiency for Industrial, IoT and automotive devices, i.MX 95 processors are built with NXP's innovative Energy Flex architecture.

The i.MX 95 applications processors offer a rich set of peripherals targeting automotive, industrial and commercial IoT market segments. As part of the EdgeVerse™ portfolio of intelligent edge solutions, the i.MX 95 family is offered in commercial, industrial, extended industrial, and automotive-level qualification, and backed by NXP's product longevity program.

The DART-MX95 provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with compact size and a very cost-effective solution.

Supporting products:

- VAR-DT8MCustomBoard – evaluation board
  - ✓ Carrier Board, compatible with DART-MX8M, DART-MX8M-MINI, DART-MX93
  - ✓ Schematics
- VAR-DVK-MX95 full development kit, including:
  - ✓ VAR-DT8MCustomBoard
  - ✓ DART-MX95
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

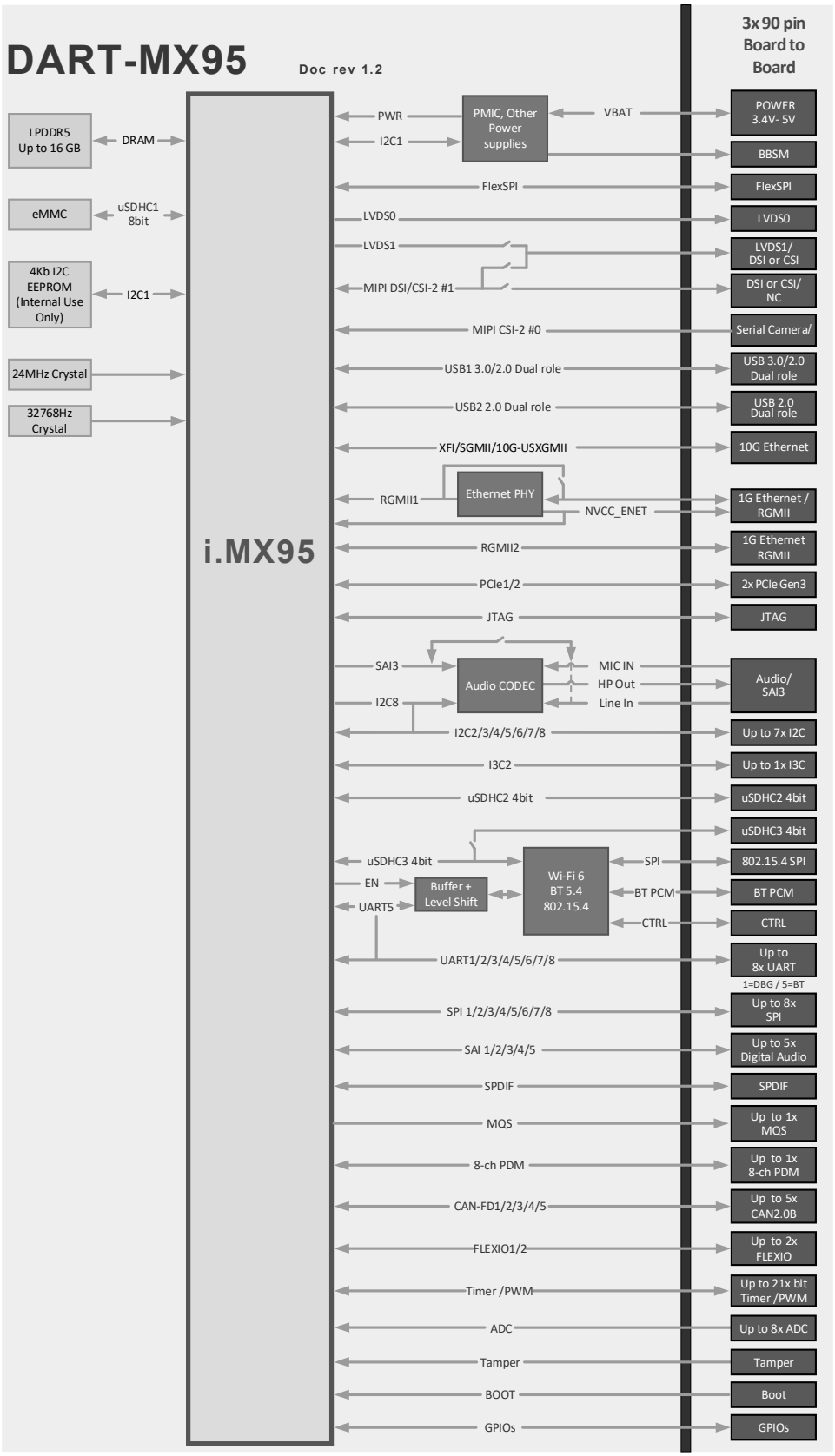
Contact Variscite support services for further information: support@variscite.com.

4.2 Feature Summary

- NXP i.MX 95 series SOC
  - 6x Arm Cortex-A55, up to 2.0 GHz frequency
  - 1x Arm Cortex-M33, up to 333 MHz frequency
  - 1x Cortex-M7, up to 800 MHz frequency
- AI/ML accelerators
  - Neural Processing Unit (NPU): Delivers up to 2.0 TOPS
- Graphics
  - 3D/2D Arm Mali-G310 Graphic Processing Unit (GPU)
- Memory
  - Up to 16GB LPDDR5 RAM Up to 6.4 GT/s
  - 8-bit up to 128GB eMMC boot and storage
- Display Support
  - Dual channel LVDS display interface Up to 1080p60
  - MIPI DSI supporting 4kp30 or 3840 x 1440p60
- Networking
  - 2x 10/100/1000 Mbit/s Ethernet Interface
  - 1x 10 Gbps Ethernet port
  - Certified Wi-Fi 802.11a/b/g/n/ac/ax
  - Bluetooth: 5.4/BLE
- Camera and ISP
  - 2x MIPI-CSI – CMOS Serial camera Interface 4 lanes (x1 muxed with DSI) with ISP
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - 5x Digital audio (SAI, SPDIF, MQS, PDM)
- USB
  - 1 x USB 3.0/2.0 Dual role, 1 x USB 2.0 Dual role
- Other Interfaces
  - SDIO/MMC
  - 2x PCIe Gen 3.0
  - Serial interfaces (LPSPI, FlexSPI, LPI2C, I3C, LPUART, FlexCAN, ADC, JTAG)
  - GPIOs
- Single power supply: 3.5V – 5V
- Dimensions (W X L x H): 30 x 55 x 4.25 [mm]
- Industrial temperature range: -40 to 85 °C

4.3 Block Diagram

Figure 1 : DART-MX95 Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the DART-MX95.

5.1 NXP i.MX 95

5.1.1 Overview

The i.MX 95 applications processor features advanced graphics and video cores, powerful vision and machine learning acceleration, efficient CPU performance, real-time processing, and advanced security with the integrated EdgeLock® secure enclave to support energy-efficient edge computing. A rich set of peripherals and processor cores support these features.

The applications processor integrates Arm® Cortex-A55, Arm® Cortex-M33, and Arm® Cortex-M7 cores. The chip supports functional safety and features NXP's innovative Energy Flex architecture to optimize performance and power efficiency.

As part of the EdgeVerse™ portfolio of intelligent edge solutions, the i.MX 95 family is offered in commercial, industrial, extended industrial, and automotive-level qualification, and backed by NXP’s product longevity program.

5.1.2 i.MX95 Block Diagram

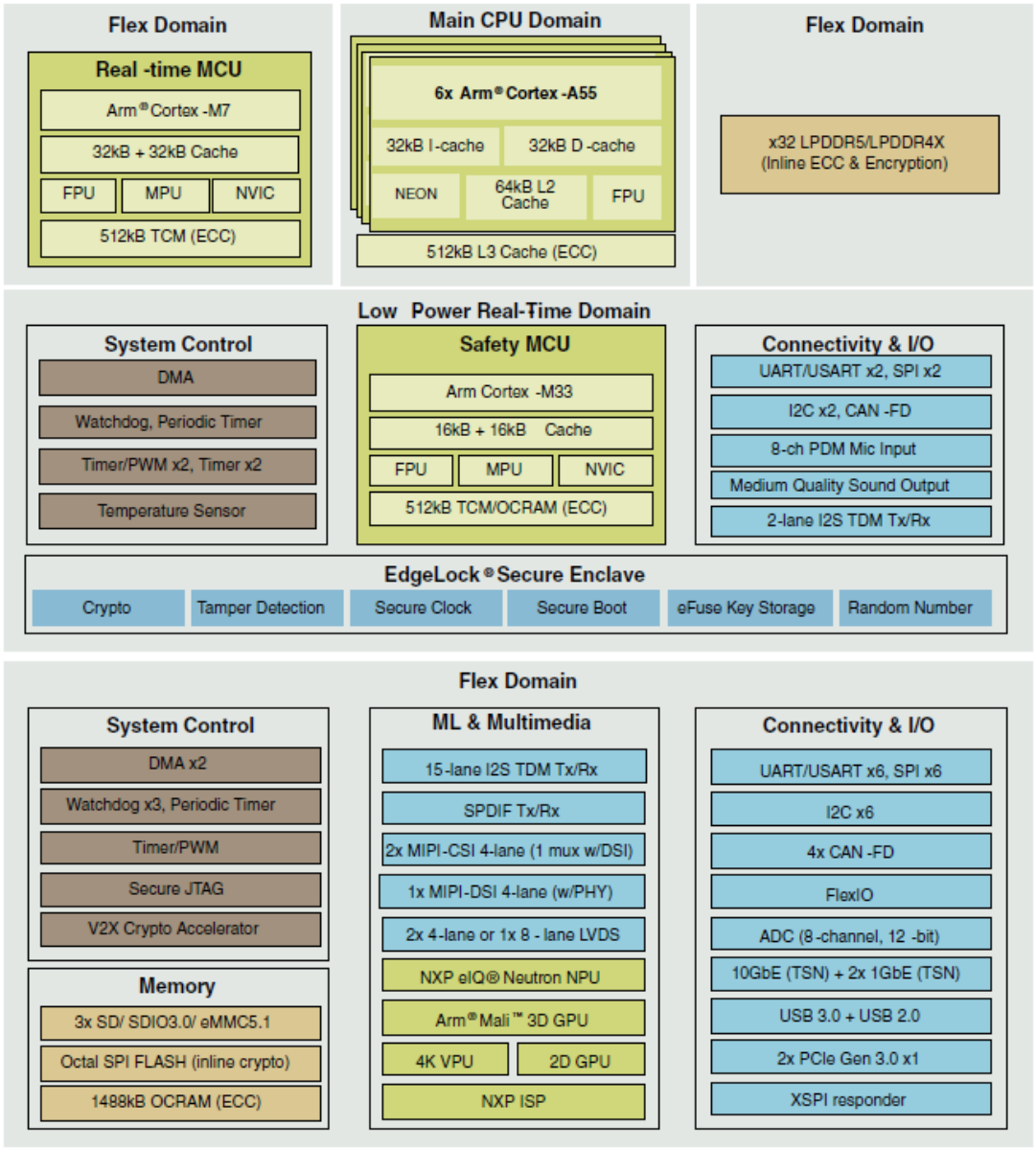


Figure 2 : iMX 95 Block Diagram

5.1.3 Arm Cortex-A55 MPCore platform

- 6 x Arm Cortex-A55
- Arm v8.2 fully 64-bit capable
- L1, L2, and L3 cache with ECC

5.1.4 Arm Cortex-M33 and Cortex-M7 platforms

- 1 x Arm Cortex-M33, up to 333 MHz frequency
- 1 x Cortex-M7, up to 800 MHz frequency
- Arm v8-M supporting Trustzone-M
- 16 KB + 16 KB (Cortex-M33) and 32 KB + 32 KB (Cortex-M7) caches (ECC)
- 512 KB (Cortex-M33) + 512 KB (Cortex-M7) TCM or on-chip SRAM (ECC)

5.1.5 Memory

- Up to 6.4 GT/s x 32 LPDDR4X/5 (with inline ECC)
- 3 x uSDHC (SD3.0, SDIO3.0, eMMC5.1)
- 8 x LPI2C
- 8 x LPSPI
- 2 x I3C
- 1 x Octal SPI, including support for SPI NOR and SPI NAND memories
- FlexSPI_FLR

5.1.6 Machine learning

High-performance NPU

5.1.7 Graphics

- Arm Mali-G310 GPU
  - 3D GPU supporting 50 GFLOPs
  - OpenGL® ES 3.2
  - Vulkan® 1.2
  - OpenCL 3.0

5.1.8 Video processors

- 4Kp30 H.265 and H.264 encode and decode
- 1 x JPEGENC
- 1 x JPEGDEC

5.1.9 Display controllers (up to three simultaneous displays)

- 1 x 350 MHz MIPI-DSI (4-lane, 2.5 Gbps/lane) supporting 4kp30 or 3840 x 1440p60
- Up to 1080p60 LVDS Tx (2 x 4-lane or 1 x 8-lane)
- 16 kByte of SRAM, but it is available for other chip usage when not using for 2D blitter purposes

5.1.10 Camera and ISP

- MIPI-CSI and ISP (2 x 4-lane, 2.5 Gbit/s per lane) with PHY (one mux'd with DSI)
- Up to 1 x 4Kp60 fps (when enabling one MIPI CSI), 2 x 4Kp30, 4 x 1080p60, or 8 x 1080p30
- Up to 8 x cameras with MIPI virtual channelsTimers

5.1.11 Audio

- 5 x SAI
- Audio XCVR PHY
- 17-lane I2S TDM (32 bit at 768 kHz frequency) Audio XCVR
- 8-channel MICFIL
- 2 x MQS

5.1.12 Connectivity

- 2 x PCIe Gen 3.0 (1-lane)
- 1 x USB 3.0 Type-C with PHY
- 1 x USB 2.0 with PHY
- 2 x 1 Gbit/s Ethernet ports with time sensitive networking (TSN) capabilities
- 1 x 10 Gbit/s Ethernet port with TSN capabilities
- IEEE 1588 for sync; and EEE
- 5 x CAN-FD
- 2 x 32-pin FLEXIO interfaces (bus or serial I/O)

5.1.13 Low-speed communication peripherals

- 8 x UART/USART/Profibus

5.1.14 Timers and PWMs

- 2 x LPIT
  - Four channels
  - Four external trigger sources
  - Generic 32-bit resolution timer
  - Periodical interrupt generation
- 6 x TPM
  - Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
  - 16-bit counter, support for free-running counter or modulo counter mode, counting up or down
  - Includes six channels that you configure for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
- 2 x LPTMR
- 5 x WDOG
- 1 x SYS_CTR
- 2 x TSTMR

5.1.15 GPIO and pin multiplexing

- GPIO modules with interrupt capability
- IOMUXC to provide centralized pad control

5.1.16 Analog

- FRO_TUNER
- 2 x TEMPSENSE
- 16-channel, 12-bit SAR_ADC
- 1 x TRGMUX to configure the trigger inputs for various peripherals

5.1.17 Clocking

- CCM
- OSC
- LPCG

5.1.18 Safety

- Integrated functional safety
- Targeting ISO26262 ASIL-B and IEC61508 SIL2 compliance

5.1.19 Security

- TRDC supports up to 16 resource domains
- Arm TrustZone® (TZ) architecture
- Secure and trusted access control
- EdgeLock™ secure enclave
- Evolved on-die security with run-time attestation, silicon root of trust, trust provisioning, and fine-grain key management augmented by extensive crypto services

5.1.20 System debug

- Arm CoreSight® debug and trace architecture
- TPIU to support off-chip real-time trace
- Support for 5-pin (JTAG) and SWD debug interfaces

5.1.21 Power management

- Support for PMIC integration to supply all power rails
- Multiple power domains that allow power gating of most digital and analog logic In Low-Power mode
- GPC: several factors are involved in power management, not just a central controller

5.2 Memory

5.2.1 RAM

The DART-MX95 is available with up to 16 GB of LPDDR5 memory capable of running up to 6400MTS.

5.2.2 Non-volatile Storage Memory

The DART-MX95 is available with a non-volatile storage memory with optional densities. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.
The DART-MX95 can arrive with up to 128GB MLC eMMC.

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- 1 fully differential mic / line input per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)

- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT + LR-WPAN

DART-MX95 module can be configured either for using one of two Wi-Fi modules based on NXP chipset:

- 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module based on NXP IW612 chipset
- 2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module based on NXP IW611 chipset

Both realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port or may be ordered with dual antenna ports.
The SOM can be ordered with 802.15.4 low-rate wireless personal area network (LR-WPAN)

DART-MX95 Wi-Fi Key Features:

- 1x1 2.4/5 GHz, up to 80 MHz channel
- UL/DL MU-MIMO and OFDMA
- Target Wake Time, Dual Carrier Modulation, Extended Range
- 802.11az accurate ranging
- WPA3 security

DART-MX95 Bluetooth Key Features:

- Supports Bluetooth 5.4
- Integrated high power PA up to +20 dBm transmit power
- Full featured Bluetooth baseband
- SCO/eSCO links with hardware accelerated audio signal processing
- Bluetooth LE 2 Mbit/s, Long Range, Advertising Extensions
- LE Audio with Isochronous channels (I2S/PCM)

DART-MX95 802.15.4 Key Features:

- IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
- Integrated high power PA up to +20 dBm transmit power
- Shared transmitter and antenna pin with Bluetooth
- Simultaneous receive with Bluetooth

5.4.1 DART-MX95 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Option

The DART-MX95 contains Murata's certified high-performance Type 2EL Module based upon the NXP IW612 chipset supporting Wi-Fi® 11a/b/g/n/ac/ax + Bluetooth® 5.4 + 802.15.4 wireless connectivity.

5.4.2 DART-MX95 2.4GHz & 5GHz Wi-Fi® + Bluetooth® Option

The DART-MX95 contains Murata's certified high-performance Type 2DL Module based upon the NXP IW611 chipset supporting Wi-Fi® 11a/b/g/n/ac/ax + Bluetooth® 5.4 wireless connectivity.

5.5 PMIC

The DART-MX95 features NXP's PMICs: PF09, PF502, PF503 as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX 95 series of application processors. The PMICS regulate all power rails required on SOM from a single power supply with 3.5V – 5V range.
The PMICs are programmable via the I2C interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6 10/100/1000 Mbps Ethernet Transceiver

The SOM features on board an MXL86110C or MXL86110I Integrated Ethernet Transceiver.

Key features include:

- 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3) and 10BASE-Te (IEEE 802.3)
- Ethernet twisted pair copper cable of category CAT5 or higher
- Low EMI voltage mode line driver with integrated termination resistors
- Transformer less Ethernet for backplane applications
- Auto-Negotiation (ANEG) with extended next page support
- Auto-MDIX and polarity correction
- Auto-Down speed (ADS)
- Energy-Efficient Ethernet (EEE) and power down mode
- Wake-on-LAN (WoL)
- 10k byte jumbo frame support
- RGMII Interface
- An MDIO slave interface supports IEEE 802.3 Clause 22 and Clause 45
- An MDIO interface clock of up to 12.5 MHz
- Three MDIO message frame types: Clause 22, Clause 22 Extended, and Clause 45
- Two fully programmable LEDs

5.7 EEPROM

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters. This EEPROM is connected to I2C1 bus and intended only for holding the above information. The SOM may not boot if the contents of EEPROM device are corrupted.

6. DART-MX95 Hardware Configuration

DART-MX95 hardware interfaces, explained on sections 5.3, 5.4 and 5.6 are configured using the orderable part number of the module.

For every hardware configuration option, the SOM pinout will be affected, see section 7.3 for complete list.

Table 1 details part of the hardware configuration orderable options.

Table 1: Partial Hardware Configuration Options

OPTION	DESCRIPTION
EC	Ethernet Controller PHY assembled on SOM
AC	Audio Codec assembled on SOM
WBE	2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module assembled on SOM
WBD	2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module assembled on SOM
BTRST	Expose Bluetooth® and 802.15.4 reset lines [1]
WRST	Expose 2.4GHz & 5GHz Wi-Fi® reset line [1]
RFCNTL	Expose 2.4GHz & 5GHz Wi-Fi® RF_CNTL lines [1]
COEX	Expose WCI-2 coexistence management lines [1]
ANT2	Dual antenna mode. ANT1 for Wi-Fi, ANT2 for BT and 802.15.4 [1]
BTPCM	Expose Bluetooth® PCM lines [1]
SDEX	SD3 lines exported in case of no Wi-Fi Module assembled
DSCM	DSI Compatibility Mode: DSI lanes exported via SOM connector pins instead of LVDS1 lanes – as in DART-MX8M and DART-MX8M-MINI; By default, DSI exported on other pins.
SPICM	WBE SPI Compatibility – WBE SPI_TXD line routed also to pin J1.63
ADC	Export ADC lines
CMP	Instead of power pins, J3.15/27/34/63 are not connected for compatibility with other DART SoMs.
xR	LPDDR5 4G/8G/16G (4/8/16 GB)
xG	eMMC Configuration size: 8G/16G/32G/64G/128G (8/16/32/64/128 GB)

NOTE

[1] This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

7. External Connectors

7.1 Board to Board Connector

- The DART-MX95 exposes three 90-pin board-to-board connectors.
- The recommended mating connector is: **Hirose Electric Co Ltd PN: DF40C-90DS-0.4V(51)**

7.2 Wi-Fi & BT Connector

- Modules with Wi-Fi ***"WBD", "WBE" Configuration -*** a combined Wi-Fi + BT antenna connector is assembled.
- In case of Modules with ***"ANT2" Configuration -*** dual Antenna connectors are assembled.
- Connector type: **U.FL JACK connector**
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 DART-MX95 Connector Pin-out

Tables under this section lists the SOM connectors pinout with each pin listed for all the available ball names related to the assembly hardware configuration options.

Table 2: PIN-OUT Tables Mnemonics

Column Heading		Meaning
PIN#	**Jx.YY**	Pin number on a connector: Jx : Can be J1 J2 or J3 YY : Can be 1 to 90
ASSY		Can be any of the **options listed in Table 1**. **"no"** - will be added to above option - means the option is not part of the SOM part number. **Blank** - pin listed have no hardware configuration option **NC** - Pin is Not Connected
BALL NAME		Name of the ball for the specific ASSY option
GPIO	**GPIOx_y**	SOC pin GPIO Alternate function number including: **x- GPIO bank** **y-Bit number in the bank**
NOTES		This column displays any special note related to the specific pin with the specific ASSY The notes will repeat also in the function tables.
BALL		Source device and it's pin number.
	XX.YY	XX: Source Chip can be: SOC.yy – pins connected to the iMX 95 SoC MxL86110x.yy – pins connected the Ethernet Controller (***"EC" Configuration***) WM8904.yy - pins connected the Audio Codec (***"AC" Configuration***) LBES5PL2xL- pins connected the Wi-Fi module (***"WBD","WBE" Configuration***) PF09.yy,PF05302.yy, PF05301.yy - pins connected the PMICs YY : Pin/Ball number of source chip.

NOTE

A. Some pins may appear in several consecutive lines if additional chip function used on SOM; Relates to the DART-MX95 orderable hardware configuration.

B. In case a chip is added due to an orderable configuration the chip function must be used.

7.3.1 DART-MX95 J1 Pin-out

Table 3: J1 PIN-OUT

Pin	Assembly	Pin name	Notes	GPIO	Ball
J1.01		PF09_INT_B_PF53_SOC_PG_PF53_ARM_PG	PF09 interrupt, PF5302 PGOOD, PF5301 PGOOD signals AND connected with internal PU (In initial SOM Rev 1.0 PF09 interrupt not connected)		PF09.41, PF5302.8, PF5301.8
J1.02	no EC	ENET1_TD1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO04	AG35
J1.02	EC	ETH_TRX1_P	Signal source is Ethernet PHY;		MxL86110x.4
J1.03	no EC	ENET1_TX_CTL	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO06	AF32
J1.03		NC	In "EC" configuration this pin is Not Connected.		NC
J1.04	no EC	ENET1_TD0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO05	AG33
J1.04	EC	ETH_TRX1_N	Signal source is Ethernet PHY;		MxL86110x.5
J1.05	no EC	ENET1_TXC	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface;	GPIO4_IO07	AG31
J1.05	EC	LED_LINK10_100	Signal source is Ethernet PHY; In "EC" configuration - connected to GND		GND
J1.06	no EC	ENET1_TD2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO03	AF36
J1.06	EC	ETH_TRX0_N	Signal source is Ethernet PHY;		MxL86110x.2
J1.07	no EC	ENET1_RXC	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface;	GPIO4_IO09	AJ33
J1.07	EC	LED_LINK1000	Signal source is Ethernet PHY; In "EC" configuration - LED, Runs@3.3V		MxL86110x.33
J1.08	no EC	ENET1_TD3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO02	AG37
J1.08	EC	ETH_TRX0_P	Signal source is Ethernet PHY;		MxL86110x.1
J1.09	no EC	ENET1_RX_CTL	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO08	AH34
J1.09	EC	LED_ACT	Signal source is Ethernet PHY; In "EC" configuration - LED, Runs@3.3V		MxL86110x.34
J1.10	no EC	ENET1_RD0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO10	AJ35
J1.10	EC	ETH_TRX2_P	Signal source is Ethernet PHY;		MxL86110x.6
J1.11		ENET1_MDIO	Runs @ 3.3V level via NTS0104GU12 level translator	GPIO4_IO01	AJ39
J1.12	no EC	ENET1_RD1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO11	AK36
J1.12	EC	ETH_TRX2_N	Signal source is Ethernet PHY;		MxL86110x.7
J1.13		ENET1_MDC	Runs @ 3.3V level via NTS0104GU12 level translator	GPIO4_IO00	AK40
J1.14	no EC	ENET1_RD2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO12	AJ37
J1.14	EC	ETH_TRX3_P	Signal source is Ethernet PHY;		MxL86110x.9
J1.15		VDD_BBSM_1V8	BBSM domain power output 1.8V		PF09.16
J1.16	no EC	ENET1_RD3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO13	AH38
J1.16	EC	ETH_TRX3_N	Signal source is Ethernet PHY;		MxL86110x.10

Pin	Assembly	Pin name	Notes	GPIO	Ball
J1.17		GPIO_IO11		GPIO2_IO11	M52
J1.18		GND			GND
J1.19		GPIO_IO10		GPIO2_IO10	M48
J1.20		ONOFF	SOC input with internal 100K PU; Runs @ VDD_BBSM_1V8 level		F40
J1.21		GND			GND
J1.22		PWRON	SoC output with 100K PD connected to PF09 PMIC PWRON input; Pull low to hold DART internal regulators OFF; Pulse low for cold reboot; Runs @ VDD_BBSM_1V8 level		PF09.28
J1.23	no WBD/WBE	NC	in "no WBD" or "no WBE" configuration this pin is Not Connected.		NC
J1.23	WBD/WBE	BT_HOST_WAKE_1V8	Signal source is WIFI module. Available in "WBD" or "WBE" configuration Output from WIFI module; Runs @ 1.8V		LBES5PL2xL.76
J1.24		POR_B_1V8	PMIC output with 100K PU connected to SOC; Can be pulled low externally to cause warm reset. Runs @ VDD_BBSM_1V8 level;		D42
J1.25	no WBD/WBE	NC	in "no WBD" or "no WBE" configuration this pin is Not Connected.		NC
J1.25	WBD/WBE	WIFI_HOST_WAKE_1V8	Signal source is WIFI module. Available in "WBD" or "WBE" configuration Output from WIFI module; Runs @ 1.8V		LBES5PL2xL.73
J1.26		PMIC_STBY_REQ_1V8	SOC output with 100K PD connected to PF09 PMIC STBY input; Can be used externally to control carrier board power for standby state; Active-high output for going to SUSPEND state; Runs @ VDD_BBSM_1V8 level		C43
J1.27		VDD_3V3	Power output from PMIC; Powers all 3.3V Ios; Recommend to use as base board 3.3V regulator enable;		PF09.49
J1.28		SD2_RST_B	Recommend using SD2_RESET_B for external SD card power cycle. Will change level according to J1.90 VDD_SDIO2;	GPIO3_IO07	AD52
J1.29	no ADC	NC			NC
J1.29	ADC	ADC_IN0	Available in "ADC" configuration; Runs @ 1.8V		A37
J1.30		GND			GND
J1.31		ETH_3V3	PF09 PMIC LDO1 output; In "EC" configuration - Ethernet PHY 3.3V power supply In "no EC" configuration - NVCC_ENET domain power supply setting ENET1/2 reference voltage: Default - 3.3V, should be set to 1.8V for ENET1/2 RGMII support Max. 200mA draw allowed;		PF09.53
J1.32		XSPI_DATA1	Runs @ 1.8V	GPIO5_IO01	AH46
J1.33		GND			GND
J1.34		XSPI_SS0_B	Runs @ 1.8V	GPIO5_IO10	AJ41
J1.35		ETH_CLKIN_N	Need to supply 156.25 MHz for 10G ETH clock reference;		AF14
J1.36	no BTPCM	NC			NC
J1.36	BTPCM	BT_PCM_IN_1V8	Signal source is WIFI module. Available In "BTPCM" configuration; Runs @ 1.8V		LBES5PL2xL.60
J1.37		ETH_CLKIN_P	Need to supply 156.25 MHz for 10G ETH clock reference;		AG15
J1.38		XSPI_DQS	Runs @ 1.8V	GPIO5_IO08	AK44
J1.39	no RFCTRL	NC			NC

Pin	Assembly	Pin name	Notes	GPIO	Ball
J1.39	RFCTRL	RF_CNTL1_1V8	Signal source is WIFI module. Available in "RFCTRL" configuration; Runs @ 1.8V		LBES5PL2xL.26
J1.40		XSPI_CLK	Runs @ 1.8V	GPIO5_IO09	AJ43
J1.41	no WBE	NC			NC
J1.41	WBE	SPI_TXD_1V8	Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V		LBES5PL2xL.7
J1.42		ETH_TX0_N			AK16
J1.43		ETH_RX0_N			AK12
J1.44		ETH_TX0_P			AJ17
J1.45		ETH_RX0_P			AJ13
J1.46		XSPI_DATA3	Runs @ 1.8V	GPIO5_IO03	AK48
J1.47		XSPI_SS1_B	Runs @ 1.8V	GPIO5_IO11	AH42
J1.48		XSPI_DATA0	Runs @ 1.8V	GPIO5_IO00	AJ45
J1.49		GND			GND
J1.50		XSPI_DATA2	Runs @ 1.8V	GPIO5_IO02	AJ47
J1.51		PCIE1_CLKIN_N	Need to supply 100MHz PCIe clock reference;		C31
J1.52	no BTRST	GND			GND
J1.52	BTRST	BT_KILL_1V8	Signal source is WIFI module. Available in "BTRST" configuration; Runs @ 1.8V		LBES5PL2xL.64
J1.53		PCIE1_CLKIN_P	Need to supply 100MHz PCIe clock reference;		B30
J1.54	no SPICM & no BTPCM & no RFCTRL	PCIE2_CLKIN_N	In "no SPICM" and "no BTPCM " and "no RFCTRL" configuration - Need to supply 100MHz PCIe clock reference;		A33
J1.54	BTPCM	BT_PCM_CLK_1V8	Signal source is WIFI module. Available in "BTPCM" configuration Runs @ 1.8V		LBES5PL2xL.57
J1.55	no WBE	GND			GND
J1.55	WBE	SPI_CS0_1V8	Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V		LBES5PL2xL.4
J1.56	no SPICM & no BTPCM & no RFCTRL	PCIE2_CLKIN_P	In "no SPICM" and "no BTPCM " and "no RFCTRL" configuration - Need to supply 100MHz PCIe clock reference;		B32
J1.56	BTPCM	BT_PCM_OUT_1V8	Signal source is WIFI module. Available in "BTPCM" configuration Runs @ 1.8V		LBES5PL2xL.59
J1.57		PCIE1_TX0_N			D30
J1.58	no WRST	GND			GND
J1.58	WRST	WB_KILL_1V8	Signal source is WIFI module. Available in "WRST" configuration; Runs @ 1.8V		LBES5PL2xL.63
J1.59		PCIE1_TX0_P			E29
J1.60		PCIE1_RX0_N			A29
J1.61	no WBE	GND			GND
J1.61	WBE	SPI_RXD_1V8	Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V		LBES5PL2xL.6
J1.62		PCIE1_RX0_P			B28
J1.63	no SPICM & no BTPCM & no RFCTRL	PCIE2_RX0_N			C35
J1.63	WBE&SPICM	SPI_TXD_1V8	Signal source is WIFI module. In "WBE and SPICM" configuration; Runs @ 1.8V		LBES5PL2xL.7
J1.64	no RFCTRL	GND			GND
J1.64	RFCTRL	RF_CNTL0_1V8	Signal source is WIFI module. Available in "RFCTRL" configuration; Runs @ 1.8V		LBES5PL2xL.27
J1.65	no SPICM & no BTPCM & no RFCTRL	PCIE2_RX0_P			B34
J1.65	BTPCM	BT_PCM_SYNC_1V8	Signal source is WIFI module. Available In "BTPCM" configuration; Runs @ 1.8V		LBES5PL2xL.61

Pin	Assembly	Pin name	Notes	GPIO	Ball
J1.66	no SPICM & no BTPCM & no RFCTRL	PCIE2_TX0_N			F32
J1.66	RFCTRL	RF_CNTL3_1V8	Signal source is WIFI module. Available in "RFCTRL" configuration; Runs @ 1.8V		LBES5PL2xL.25
J1.67	no WBE	GND			GND
J1.67	WBE	SPI_CLK_1V8	Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V		LBES5PL2xL.8
J1.68	no SPICM & no BTPCM & no RFCTRL	PCIE2_TX0_P			E31
J1.68	RFCTRL	RF_CNTL4_1V8	Signal source is WIFI module. Available in "RFCTRL" configuration; Runs @ 1.8V		LBES5PL2xL.24
J1.69		MIPI_CSI_D3_P			E11
J1.70	no BTRST	GND			GND
J1.70	BTRST	LR_KILL_1V8	Signal source is WIFI module. Available in "BTRST" configuration; Runs @ 1.8V		LBES5PL2xL.38
J1.71		MIPI_CSI_D3_N			F12
J1.72		SAI1_TXD_BT_MODE3	Duplicate pin on J2.44 BOOT_MODE3 pin, Has internal 10K PU to J1.27 (3.3V); Do not drive until after POR_B rise + 30ms; GPIO can be output only or tristated.	GPIO1_IO13	H48
J1.73		MIPI_CSI_D1_P			E17
J1.74		SD2_CD_B	External SD card detect input; Add 10K external pull up to J1.90; Will change level according to J1.90 VDD_SDIO2;	GPIO3_IO00	AD48
J1.75		MIPI_CSI_D1_N			D18
J1.76		GND			GND
J1.77		MIPI_CSI_D2_N			D14
J1.78		SD2_DATA2	Will change level according to J1.90 VDD_SDIO2;	GPIO3_IO05	AA51
J1.79		MIPI_CSI_D2_P			E13
J1.80		SD2_DATA1	Will change level according to J1.90 VDD_SDIO2;	GPIO3_IO04	AC49
J1.81		MIPI_CSI_D0_P			E19
J1.82		SD2_CLK	Will change level according to J1.90 VDD_SDIO2;	GPIO3_IO01	AB48
J1.83		MIPI_CSI_D0_N			F20
J1.84		SD2_DATA3	Will change level according to J1.90 VDD_SDIO2;	GPIO3_IO06	AA49
J1.85		GND			GND
J1.86		SD2_DATA0	Will change level according to J1.90 VDD_SDIO2;	GPIO3_IO03	AC51
J1.87		MIPI_CSI_CLK_P			E15
J1.88		SD2_CMD	Will change level according to J1.90 VDD_SDIO2;	GPIO3_IO02	AB52
J1.89		MIPI_CSI_CLK_N			F16
J1.90		VDD_SDIO2	Power output for SD2 pins reference 1.8V/3.3V- set by DART PMIC;		PF09.3

7.3.2 DART-MX95 J2 Pin-out

Table 4: J2 PIN-OUT

Pin	Assembly	Pin name	Notes	GPIO	Ball
J2.01		JTAG_TCK	Add external 10K pull down; Runs @ 1.8V		AG21
J2.02	no AC	GPIO_IO20		GPIO2_IO20	R49
J2.02	AC	HPLOUT	Signal source is Audio Codec; Left headphone output (line or headphone output). 100nF and 20Ω Zobel network required		WM8904.13
J2.03		JTAG_TMS	Runs @ 1.8V		AH22
J2.04	no AC	GPIO_IO16		GPIO2_IO16	P46
J2.04	AC	HPROUT	Signal source is Audio Codec; Right headphone output (line or headphone output). 100nF and 20Ω Zobel network required		WM8904.15
J2.05	no ADC	NC			NC
J2.05	ADC	ADC_IN7	Available in "ADC" configuration Runs @ 1.8V		A45
J2.06	no AC	GPIO_IO19		GPIO2_IO19	R45
J2.06	AC	HPOUTFB	Signal source is Audio Codec; Headphone output ground loop noise rejection feedback;		WM8904.14
J2.07		JTAG_TDI	Runs @ 1.8V		AK24
J2.08	no AC	GPIO_IO18		GPIO2_IO18	P52
J2.08	AC	LINEIN1_LP	Signal source is Audio Codec; Left channel input;		WM8904.26
J2.09		JTAG_TDO	Runs @ 1.8V		AJ23
J2.10	no AC	GPIO_IO26		GPIO2_IO26	U45
J2.10	AC	LINEIN1_RP	Signal source is Audio Codec; Right channel input;		WM8904.24
J2.11		UART2_TXD_BT_MODE1	Duplicate pin on J3.50 (In initial SOM Rev 1.0 on pin J3.48); BOOT_MODE1 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull up to J1.27 (3.3V); GPIO can be output only or tristated.	GPIO1_IO07	F48
J2.12		AGND	Connect to GND;		AGND
J2.13		SAI1_TXFS_BT_MODE2	Duplicate pin on J2.42 BOOT_MODE2 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull down; GPIO can be output only or tristated.	GPIO1_IO11	G49
J2.14	no AC	GPIO_IO21		GPIO2_IO21	R51
J2.14	AC	DMIC_CLK	Signal source is Audio Codec; DMIC output 3.3V level;		WM8904.01
J2.15	no ADC	NC			NC
J2.15	ADC	ADC_IN1	Available in "ADC" configuration Runs @ 1.8V		B38
J2.16	no AC	GPIO_IO17		GPIO2_IO17	P48
J2.16	AC	DMIC_DATA	Signal source is Audio Codec; DMIC input is 1.8V level; Add ~500 Ohm voltage divider;		WM8904.27
J2.17	no ADC	NC			NC
J2.17	ADC	ADC_IN2	Available in "ADC" configuration Runs @ 1.8V		C39
J2.18		GND			GND
J2.19		NC			NC
J2.20		GPIO_IO00	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage;	GPIO2_IO00	J49

Pin	Assembly	Pin name	Notes	GPIO	Ball
J2.21		NC			NC
J2.22		GPIO_IO03	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage;	GPIO2_IO03	K52
J2.23		GND			GND
J2.24		GPIO_IO01	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage;	GPIO2_IO01	J51
J2.25		AUD_P_UTIL			Y44
J2.26		GPIO_IO02	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage;	GPIO2_IO02	K48
J2.27		AUD_N_HPD			Y46
J2.28		WDOG_ANY	Recommend using as WDOG_ANY to cold reset the DART with internal watch dog event;	GPIO1_IO15	J45
J2.29	no SDEX	NC			NC
J2.29	SDEX	CONN_SD3_DATA3	Available in "SDEX" configuration; Runs @ 1.8V	GPIO3_IO25	AF52
J2.30		GPIO_IO28		GPIO2_IO28	U51
J2.31	no SDEX	NC			NC
J2.31	SDEX	CONN_SD3_DATA2	Available in "SDEX" configuration; Runs @ 1.8V	GPIO3_IO24	AE49
J2.32		GPIO_IO29		GPIO2_IO29	V44
J2.33	no SDEX	NC			NC
J2.33	SDEX	CONN_SD3_DATA1	Available in "SDEX" configuration; Runs @ 1.8V	GPIO3_IO23	AH52
J2.34		I2C2_SCL		GPIO1_IO02	E43
J2.35	no SDEX	NC			NC
J2.35	SDEX	CONN_SD3_DATA0	Available in "SDEX" configuration; Runs @ 1.8V	GPIO3_IO22	AG49
J2.36		SAI1_RXD		GPIO1_IO14	H52
J2.37	no COEX	NC			NC
J2.37	COEX	COEX_SIN_1V8	Signal source is WIFI module. Available in "COEX" configuration; Runs @ 1.8V		LBES5PL2xL.69
J2.38		SAI1_TXC		GPIO1_IO12	G51
J2.39	no COEX	NC			NC
J2.39	COEX	COEX_SOUT_1V8	Signal source is WIFI module. Available in "COEX" configuration; Runs @ 1.8V		LBES5PL2xL.70
J2.40		I2C2_SDA		GPIO1_IO03	E45
J2.41		VDD_1V8	1.8V Power output from PMIC; Powers all 1.8V Ios		PF09.21
J2.42		SAI1_TXFS_BT_MODE2	Duplicate pin on J2.13; see J2.13 note	GPIO1_IO11	G49
J2.43	no SDEX	NC			NC
J2.43	SDEX	CONN_SD3_CMD	Available in "SDEX" configuration; Runs @ 1.8V	GPIO3_IO21	AF48
J2.44		SAI1_TXD_BT_MODE3	Duplicate pin on J1.72; see J1.72 note	GPIO1_IO13	H48
J2.45	no SDEX	NC			NC
J2.45	SDEX	CONN_SD3_CLK	Available in "SDEX" configuration; Runs @ 1.8V	GPIO3_IO20	AG51
J2.46		UART2_RXD		GPIO1_IO06	E51
J2.47		GND			GND
J2.48		PDM_BIT_STREAM1		GPIO1_IO10	H46
J2.49		TAMPER0	Runs @ VDD_BBSM_1V8 level		F36
J2.50		PDM_CLK		GPIO1_IO08	F46
J2.51		TAMPER1	Runs @ VDD_BBSM_1V8 level		D38
J2.52	no WBD/WBE	NC	in "no WBD" or "no WBE" configuration this pin is Not Connected.		NC
J2.52	WBD/WBE	BT_DEV_WAKE_1V8	Signal source is WIFI module. Available in "WBD" or "WBE" configuration Input to WIFI module; Runs @ 1.8V		LBES5PL2xL.75

Pin	Assembly	Pin name	Notes	GPIO	Ball
J2.53		GND			GND
J2.54		GPIO_IO23	Duplicate pin on J3.36	GPIO2_IO23	T46
J2.55		XSPI_DATA4	Runs @ 1.8V	GPIO5_IO04	AJ49
J2.56		PDM_BIT_STREAM0		GPIO1_IO09	G45
J2.57		XSPI_DATA5	Runs @ 1.8V	GPIO5_IO05	AK50
J2.58	no ADC	NC			NC
J2.58	ADC	ADC_IN3	Available in "ADC" configuration; Runs @ 1.8V		B40
J2.59		XSPI_DATA6	Runs @ 1.8V	GPIO5_IO06	AJ51
J2.60		GPIO_IO22	Duplicate pin on J3.28	GPIO2_IO22	T44
J2.61		XSPI_DATA7	Runs @ 1.8V	GPIO5_IO07	AH50
J2.62		ENET2_MDIO	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO15	AJ31
J2.63		ENET2_MDC	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO14	AK32
J2.64		ENET2_RX_CTL	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO22	AH26
J2.65		ENET2_RD0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO24	AJ27
J2.66		ENET2_RD2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO26	AJ29
J2.67		ENET2_TD1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO18	AG27
J2.68		ENET2_RD3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO27	AH30
J2.69		ENET2_RD1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO25	AK28
J2.70		ENET2_TD0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO19	AG25
J2.71		ENET2_TXC	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO21	AG23
J2.72		ENET2_RXC	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO23	AJ25
J2.73		ENET2_TD3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO16	AG29
J2.74		ENET2_TX_CTL	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	GPIO4_IO20	AF24
J2.75		GND			GND
J2.76		CCM_CLKO1	Runs @ 1.8V		AH20
J2.77		GPIO_IO07		GPIO2_IO07	L51
J2.78		ENET2_TD2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); Internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise. This sets boot source.	GPIO4_IO17	AF28
J2.79		GPIO_IO04		GPIO2_IO04	K46

Pin	Assembly	Pin name	Notes	GPIO	Ball
J2.80		CCM_CLKO2	Runs @ 1.8V	GPIO3_IO27	AF20
J2.81		GPIO_IO05		GPIO2_IO05	L45
J2.82	no EC	NC			NC
J2.82	EC	ETH_INT_1V8	Signal source is Ethernet PHY; Available in "EC" configuration; Runs @ 1.8V		MxL86110x.31
J2.83		GPIO_IO06		GPIO2_IO06	L49
J2.84		GND			GND
J2.85		GPIO_IO13		GPIO2_IO13	N49
J2.86		GPIO_IO12		GPIO2_IO12	N45
J2.87		GPIO_IO15		GPIO2_IO15	P44
J2.88		UART1_RXD	Used as console debug on Variscite release;	GPIO1_IO04	E49
J2.89		GPIO_IO14		GPIO2_IO14	N51
J2.90		UART1_TXD_BT_MODE0	Used as console debug on Variscite release; BOOT_MODE0 pin, Do not drive until after POR_B rise + 30ms; Internal buffer connected to J2.78 drives this pin, latched with POR_B rise; This sets boot source. GPIO can be output only or tristated.	GPIO1_IO5	F52

7.3.3 DART-MX95 J3 Pin-out

Table 4: J3 PIN-OUT

Pin	Assembly	Pin name	Notes	GPIO	Ball
J3.01		GPIO_IO08		GPIO2_IO08	M44
J3.02		LVDS0_D0_P			G7
J3.03		GPIO_IO09		GPIO2_IO09	M46
J3.04		LVDS0_D0_N			G9
J3.05		LVDS0_D2_P			D6
J3.06		LVDS0_D1_P			F6
J3.07		LVDS0_D2_N			E7
J3.08		LVDS0_D1_N			F8
J3.09		GND			GND
J3.10		GND			GND
J3.11		LVDS0_CLK_P			B4
J3.12	no DSCM	LVDS1_D0_P			B2
J3.12	DSCM	DSICSI_D0_P	Two alternative locations exist!		B14
J3.13		LVDS0_CLK_N			A5
J3.14	no DSCM	LVDS1_D0_N			A3
J3.14	DSCM	DSICSI_D0_N	Two alternative locations exist!		C15
J3.15	no CMP	VBAT	In CMP configuration this pin is not connected,		VBAT
J3.15	CMP	NC			NC
J3.16	no DSCM	LVDS1_D1_P			C1
J3.16	DSCM	DSICSI_D1_P	Two alternative locations exist!		B12
J3.17		LVDS0_D3_P			D8
J3.18	no DSCM	LVDS1_D1_N			C3
J3.18	DSCM	DSICSI_D1_N	Two alternative locations exist!		A13
J3.19		LVDS0_D3_N			E9
J3.20	no DSCM	LVDS1_D3_P			F2
J3.20	DSCM	DSICSI_D3_P	Two alternative locations exist!		B6
J3.21		GND			GND
J3.22	no DSCM	LVDS1_D3_N			F4
J3.22	DSCM	DSICSI_D3_N	Two alternative locations exist!		C7

Pin	Assembly	Pin name	Notes	GPIO	Ball
J3.23	no DSCM	LVDS1_CLK_P			D2
J3.23	DSCM	DSICSI_D2_P	Two alternative locations exist!		B8
J3.24		GND			GND
J3.25	no DSCM	LVDS1_CLK_N			D4
J3.25	DSCM	DSICSI_D2_N	Two alternative locations exist!		A9
J3.26		USB2_VBUS	5V tolerant; VBUS detect input		E27
J3.27	no CMP	VBAT	In CMP configuration this pin is not connected,		VBAT
J3.27	CMP	NC			NC
J3.28		GPIO_IO22	Duplicate pin on J2.60	GPIO2_IO22	T44
J3.29	no DSCM	LVDS1_D2_N			E3
J3.29	DSCM	DSICSI_CLK_N	Two alternative locations exist!		C11
J3.30	no ADC	NC			NC
J3.30	ADC	ADC_IN4	Available in "ADC" configuration; Runs @ 1.8V		A41
J3.31	no DSCM	LVDS1_D2_P			E1
J3.31	DSCM	DSICSI_CLK_P	Two alternative locations exist!		B10
J3.32	no WBE	NC			NC
J3.32	WBE	SPI_INT_1V8	Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V		LBES5PL2xL.5
J3.33		GND			GND
J3.34	no CMP	VBAT	In CMP configuration this pin is not connected,		VBAT
J3.34	CMP	NC			NC
J3.35		USB1_RX1_N			A17
J3.36		GPIO_IO23	Duplicate pin on J2.54	GPIO2_IO23	T46
J3.37		USB1_RX1_P			B16
J3.38		GPIO_IO32		GPIO5_IO12	V52
J3.39		GND			GND
J3.40	no ADC	NC			NC
J3.40	ADC	ADC_IN5	Available in "ADC" configuration; Runs @ 1.8V		B42
J3.41		USB1_TX1_N			D22
J3.42		GPIO_IO30	Pin has 4.99K pull up on DART	GPIO2_IO30	V46
J3.43		USB1_TX1_P			E21
J3.44		USB2_ID	USB2 PHY native ID analog input; No GPIO function; Usage not recommended; NXP recommends using any GPIO to implement OTG function.		F24
J3.45		GND			GND
J3.46		GPIO_IO31	Pin has 4.99K pull up on DART	GPIO2_IO31	V48
J3.47		USB2_DP	USB OTG signal		B24
J3.48		GPIO_IO33	(In initial SOM Rev 1.0 exported on pin J3.50)	GPIO5_IO13	W45
J3.49		USB2_DN	USB OTG signal		A25
J3.50		UART2_TXD_BT_MODE1	Duplicate pin on J2.11; see J2.11 note (In initial SOM Rev 1.0 exported on pin J3.48)	GPIO1_IO07	F48
J3.51		GND			GND
J3.52		GPIO_IO34		GPIO5_IO14	W49
J3.53		USB1_RX0_N			B20
J3.54		GPIO_IO24		GPIO2_IO24	T48
J3.55		USB1_RX0_P			A21
J3.56		USB1_ID	USB1 PHY native ID analog input; No GPIO function; Usage not recommended; NXP recommends using any GPIO to implement OTG function.		C23
J3.57		GND			GND
J3.58		GPIO_IO35		GPIO5_IO15	W51
J3.59		USB1_TX0_N			E25
J3.60	no ADC	NC			NC

Pin	Assembly	Pin name	Notes	GPIO	Ball
J3.60	ADC	ADC_IN6	Available in "ADC" configuration; Runs @ 1.8V		B44
J3.61		USB1_TX0_P			D26
J3.62		GPIO_IO37		GPIO5_IO17	Y52
J3.63	no CMP	VBAT	In CMP configuration this pin is not connected,		VBAT
J3.63	CMP	NC			NC
J3.64		GPIO_IO25		GPIO2_IO25	T52
J3.65		USB1_DP	USB OTG signal		C19
J3.66		USB1_VBUS	5V tolerant; VBUS detect input		E23
J3.67		USB1_DN	USB OTG signal		B18
J3.68		GND			GND
J3.69		NC			NC
J3.70	no DSCM	DSICSI_CLK_N	Two alternative locations exist!		C11
J3.70	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.71		VBAT			VBAT
J3.72	no DSCM	DSICSI_CLK_P	Two alternative locations exist!		B10
J3.72	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.73		VBAT			VBAT
J3.74		GND			GND
J3.75		VBAT			VBAT
J3.76	no DSCM	DSICSI_D3_N	Two alternative locations exist!		C7
J3.76	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.77		VBAT			VBAT
J3.78	no DSCM	DSICSI_D3_P	Two alternative locations exist!		B6
J3.78	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.79		VBAT			VBAT
J3.80	no DSCM	DSICSI_D1_N	Two alternative locations exist!		A13
J3.80	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.81		VBAT			VBAT
J3.82	no DSCM	DSICSI_D1_P	Two alternative locations exist!		B12
J3.82	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.83		VBAT			VBAT
J3.84	no DSCM	DSICSI_D0_N	Two alternative locations exist!		C15
J3.84	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.85		VBAT			VBAT
J3.86	no DSCM	DSICSI_D0_P	Two alternative locations exist!		B14

Pin	Assembly	Pin name	Notes	GPIO	Ball
J3.86	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.87		VBAT			VBAT
J3.88	no DSCM	DSICSI_D2_N	Two alternative locations exist!		A9
J3.88	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC
J3.89		VBAT			VBAT
J3.90	no DSCM	DSICSI_D2_P	Two alternative locations exist!		B8
J3.90	DSCM	NC	In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM		NC

7.4 DART-MX95 Pin-Mux

This section tables lists the SOM connectors with the available functions on each pin.

Table 5: DART-MX95_J1 PINMUX

Pin	Assembly	Ball	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J1.02	no EC	AG35	netc.ETH0_RGMII_TXD[1]	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC	flexio2.FLEXIO[4]	gpio4.IO[4]	i3c2.PUR_B	netc.ETH0_RMII_TXD[1]
J1.03	no EC	AF32	netc.ETH0_RGMII_TX_CTL	uart3.DTR_B	netc.ETH0_RMII_TX_EN		flexio2.FLEXIO[6]	gpio4.IO[6]		
J1.04	no EC	AG33	netc.ETH0_RGMII_TXD[0]	uart3.TX	netc.ETH0_RMII_TXD[0]		flexio2.FLEXIO[5]	gpio4.IO[5]		
J1.05	no EC	AG31	netc.ETH0_RGMII_TX_CLK	ccmsrcgpcmix.ENET_REF_CLK_ROOT			flexio2.FLEXIO[7]	gpio4.IO[7]		
J1.06	no EC	AF36	netc.ETH0_RGMII_TXD[2]	INPUT=netc.ETH0_RMII_REF50_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT	can2.RX	usb2.OTG_OC	flexio2.FLEXIO[3]	gpio4.IO[3]		
J1.07	no EC	AJ33	netc.ETH0_RGMII_RX_CLK	netc.ETH0_RMII_RX_ER			flexio2.FLEXIO[9]	gpio4.IO[9]		
J1.08	no EC	AG37	netc.ETH0_RGMII_TXD[3]		can2.TX	usb2.OTG_ID	flexio2.FLEXIO[2]	gpio4.IO[2]		
J1.09	no EC	AH34	netc.ETH0_RGMII_RX_CTL	uart3.DSR_B	netc.ETH0_RMII_CRS_DV	usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]		
J1.10	no EC	AJ35	netc.ETH0_RGMII_RXD[0]	uart3.RX	netc.ETH0_RMII_RXD[0]		flexio2.FLEXIO[10]	gpio4.IO[10]		
J1.11		AJ39	netc.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]		
J1.12	no EC	AK36	netc.ETH0_RGMII_RXD[1]	uart3.CTS_B	netc.ETH0_RMII_RXD[1]	lptmr2.ALT0	flexio2.FLEXIO[11]	gpio4.IO[11]		
J1.13		AK40	netc.MDC	uart3.DCD_B	i3c2.SCL		flexio2.FLEXIO[0]	gpio4.IO[0]		
J1.14	no EC	AJ37	netc.ETH0_RGMII_RXD[2]		netc.ETH0_RMII_RX_ER	lptmr2.ALT1	flexio2.FLEXIO[12]	gpio4.IO[12]		
J1.16	no EC	AH38	netc.ETH0_RGMII_RXD[3]			lptmr2.ALT2	flexio2.FLEXIO[13]	gpio4.IO[13]		
J1.17		M52	gpio2.IO[11]	spi3.SCK			tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]
J1.19		M48	gpio2.IO[10]	spi3.SOUT			tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]
J1.20		F40	bbsmmix.ONOFF							
J1.24		D42	bbsmmix.POR_B							
J1.26		C43	ccmsrcgpcmix.PMIC_STBY_REQ							

Pin	Assembly	Ball	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J1.28		AD52	usdhc2.RESET_B	lptmr2.ALT1		netc.TMR_1588_GCLK	flexio1.FLEXIO[7]	gpio3.IO[7]		
J1.32		AH46	flexspi.A_DATA[1]	sai2.TX_DATA[5]	sai4.TX_SYNC	sai4.TX_DATA[1]	xspi_slv.DATA[1]	gpio5.IO[1]		
J1.34		AJ41	flexspi.A_SS0_B	sai2.RX_DATA[5]	sai4.RX_BCLK		xspi_slv.CS	gpio5.IO[10]		
J1.38		AK44	flexspi.A_DQS	sai5.RX_SYNC	sai5.TX_DATA[2]	sai2.RX_DATA[6]	xspi_slv.DQS	gpio5.IO[8]		
J1.40		AJ43	flexspi.A_SCLK	sai2.RX_DATA[4]	sai4.RX_SYNC		xspi_slv.CLK	gpio5.IO[9]		
J1.46		AK48	flexspi.A_DATA[3]	sai2.TX_DATA[7]	sai4.RX_DATA[0]		xspi_slv.DATA[3]	gpio5.IO[3]		
J1.47		AH42	flexspi.A_SS1_B	sai5.RX_BCLK	sai5.TX_DATA[3]	sai2.RX_DATA[7]		gpio5.IO[11]		
J1.48		AJ45	flexspi.A_DATA[0]	sai2.TX_DATA[4]	sai4.TX_BCLK	sai4.RX_DATA[1]	xspi_slv.DATA[0]	gpio5.IO[0]		
J1.50		AJ47	flexspi.A_DATA[2]	sai2.TX_DATA[6]	sai4.TX_DATA[0]		xspi_slv.DATA[2]	gpio5.IO[2]		
J1.72		H48	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]		
J1.74		AD48	usdhc2.CD_B	netc.TMR_1588_TRIG1	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]		
J1.78		AA51	usdhc2.DATA2	netc.TMR_1588_PP3	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]		
J1.80		AC49	usdhc2.DATA1	netc.TMR_1588_CLK	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]		
J1.82		AB48	usdhc2.CLK	netc.TMR_1588_PP1	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]	ccmsrcgpcmix.OBSERVE1	
J1.84		AA49	usdhc2.DATA3	lptmr2.ALT0	mqs2.LEFT	netc.TMR_1588_ALARM1	flexio1.FLEXIO[6]	gpio3.IO[6]		
J1.86		AC51	usdhc2.DATA0	netc.TMR_1588_PP2	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]	ccmsrcgpcmix.OBSERVE3	
J1.88		AB52	usdhc2.CMD	netc.TMR_1588_TRIG2	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]	ccmsrcgpcmix.OBSERVE2	

Table 6: DART-MX95_J2 PINMUX

Pin	Assembly	Ball	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J2.01		AG21	dap.TCLK_SWCLK		can4.RX		flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B	
J2.02	no AC	R49	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]		spi5.SOUT	spi4.SOUT	tpm3.CH1	flexio1.FLEXIO[20]
J2.03		AH22	dap.TMS_SWDIO		can4.TX		flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B	
J2.04	no AC	P46	gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]		uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]
J2.06	no AC	R45	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	flexio1.FLEXIO[19]	spi5.SIN	spi4.SIN	tpm6.CH2	sai3.TX_DATA[0]
J2.07		AK24	dap.TDI	mqs2.LEFT	netc.TMR_1588_ALARM1	can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX	
J2.08	no AC	P52	gpio2.IO[18]	sai3.RX_BCLK			spi5.PCS0	spi4.PCS0	tpm5.CH2	flexio1.FLEXIO[18]
J2.09		AJ23	dap.TDO_TRACESWO	mqs2.RIGHT	netc.TMR_1588_ALARM2	can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX	
J2.10	no AC	U45	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	flexio1.FLEXIO[26]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC
J2.11		F48	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]		
J2.13		G49	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]		
J2.14	no AC	R51	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	flexio1.FLEXIO[21]	spi5.SCK	spi4.SCK	tpm4.CH1	sai3.RX_BCLK
J2.16	no AC	P48	gpio2.IO[17]	sai3.MCLK			uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]
J2.20		J49	gpio2.IO[0]	i2c3.SDA			spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]
J2.22		K52	gpio2.IO[3]	i2c4.SCL			spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]
J2.24		J51	gpio2.IO[1]	i2c3.SCL			spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]
J2.26		K48	gpio2.IO[2]	i2c4.SDA			spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]
J2.28		J45	wdog1.WDOG_ANY	fccu.eout1				gpio1.IO[15]		
J2.29	SDEX	AF52	usdhc3.DATA3	flexspi.A_DATA[3]	sai5.RX_DATA[3]	sai5.TX_BCLK	flexio1.FLEXIO[25]	gpio3.IO[25]	xspi_slv.DATA[3]	

Pin	Assembly	Ball	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J2.30		U51	gpio2.IO[28]	i2c3.SDA	can3.TX					flexio1.FLEXIO[28]
J2.31	SDEX	AE49	usdhc3.DATA2	flexspi.A_DATA[2]	sai5.RX_DATA[2]	sai5.TX_SYNC	flexio1.FLEXIO[24]	gpio3.IO[24]	xspi_slv.DATA[2]	
J2.32		V44	gpio2.IO[29]	i2c3.SCL	can3.RX					flexio1.FLEXIO[29]
J2.33	SDEX	AH52	usdhc3.DATA1	flexspi.A_DATA[1]	sai5.RX_DATA[1]	sai5.TX_DATA[0]	flexio1.FLEXIO[23]	gpio3.IO[23]	xspi_slv.DATA[1]	
J2.34		E43	i2c2.SCL	i3c1.PUR	uart2.DCD_B	tpm2.CH2	sai1.RX_SYNC	gpio1.IO[2]	i3c1.PUR_B	
J2.35	SDEX	AG49	usdhc3.DATA0	flexspi.A_DATA[0]	sai5.TX_DATA[3]	sai5.RX_BCLK	flexio1.FLEXIO[22]	gpio3.IO[22]	xspi_slv.DATA[0]	
J2.36		H52	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]		
J2.38		G51	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]		
J2.40		E45	i2c2.SDA		uart2.RIN_B	tpm2.CH3	sai1.RX_BCLK	gpio1.IO[3]		
J2.42		G49	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]		
J2.43	SDEX	AF48	usdhc3.CMD	flexspi.A_SS0_B	sai5.TX_DATA[2]	sai5.RX_SYNC	flexio1.FLEXIO[21]	gpio3.IO[21]	xspi_slv.CS	
J2.44		H48	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]		
J2.45	SDEX	AG51	usdhc3.CLK	flexspi.A_SCLK	sai5.TX_DATA[1]	sai5.RX_DATA[0]	flexio1.FLEXIO[20]	gpio3.IO[20]	xspi_slv.CLK	
J2.46		E51	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]		
J2.48		H46	pdm.BIT_STREAM[1]	m33.NMI	spi2.PCS1	tpm2.EXTCLK	lptmr1.ALT2	gpio1.IO[10]	ccmsrcgpcmix.EXT_CLK1	
J2.49		F36	bbsmmix.TAMPER0							
J2.50		F46	pdm.CLK	mqs1.LEFT			lptmr1.ALT0	gpio1.IO[8]	can1.TX	
J2.51		D38	bbsmmix.TAMPER1							
J2.54		T46	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	can5.RX	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]
J2.55		AJ49	flexspi.A_DATA[4]	sai5.TX_DATA[0]	sai5.RX_DATA[1]		xspi_slv.DATA[4]	gpio5.IO[4]		
J2.56		G45	pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT1	gpio1.IO[9]	can1.RX	
J2.57		AK50	flexspi.A_DATA[5]	sai5.TX_SYNC	sai5.RX_DATA[2]	sai2.RX_DATA[6]	xspi_slv.DATA[5]	gpio5.IO[5]		
J2.59		AJ51	flexspi.A_DATA[6]	sai5.TX_BCLK	sai5.RX_DATA[3]	sai2.RX_DATA[7]	xspi_slv.DATA[6]	gpio5.IO[6]		
J2.60		T44	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	can5.TX	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]
J2.61		AH50	flexspi.A_DATA[7]	sai5.RX_DATA[0]	sai5.TX_DATA[1]		xspi_slv.DATA[7]	gpio5.IO[7]		
J2.62		AJ31	netc.MDIO	uart4.RIN_B	sai2.RX_BCLK		flexio2.FLEXIO[15]	gpio4.IO[15]		

Pin	Assembly	Ball	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J2.63		AK32	netc.MDC	uart4.DCD_B	sai2.RX_SYNC		flexio2.FLEXIO[14]	gpio4.IO[14]		
J2.64		AH26	netc.ETH1_RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]		flexio2.FLEXIO[22]	gpio4.IO[22]	netc.ETH1_RMII_CRS_DV	
J2.65		AJ27	netc.ETH1_RGMII_RXD[0]	uart4.RX	sai2.TX_DATA[2]	sai4.RX_BCLK	flexio2.FLEXIO[24]	gpio4.IO[24]	netc.ETH1_RMII_RXD[0]	
J2.66		AJ29	netc.ETH1_RGMII_RXD[2]	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT	flexio2.FLEXIO[26]	gpio4.IO[26]	netc.ETH1_RMII_RX_ER	
J2.67		AG27	netc.ETH1_RGMII_TXD[1]	uart4.RTS_B	sai2.RX_DATA[2]	sai4.TX_BCLK	flexio2.FLEXIO[18]	gpio4.IO[18]	netc.ETH1_RMII_TXD[1]	
J2.68		AH30	netc.ETH1_RGMII_RXD[3]	spdif1.OUT	spdif1.IN	mqs2.LEFT	flexio2.FLEXIO[27]	gpio4.IO[27]		
J2.69		AK28	netc.ETH1_RGMII_RXD[1]	spdif1.IN	sai2.TX_DATA[3]	sai4.RX_DATA[0]	flexio2.FLEXIO[25]	gpio4.IO[25]	netc.ETH1_RMII_RXD[1]	
J2.70		AG25	netc.ETH1_RGMII_TXD[0]	uart4.TX	sai2.RX_DATA[3]	sai4.TX_DATA[0]	flexio2.FLEXIO[19]	gpio4.IO[19]	netc.ETH1_RMII_TXD[0]	
J2.71		AG23	netc.ETH1_RGMII_TX_CLK	ccmsrcgpcmix.ENET_REF_CLK_ROOT	sai2.TX_BCLK		flexio2.FLEXIO[21]	gpio4.IO[21]		
J2.72		AJ25	netc.ETH1_RGMII_RX_CLK	netc.ETH1_RMII_RX_ER	sai2.TX_DATA[1]	sai4.RX_SYNC	flexio2.FLEXIO[23]	gpio4.IO[23]		
J2.73		AG29	netc.ETH1_RGMII_TXD[3]		sai2.RX_DATA[0]		flexio2.FLEXIO[16]	gpio4.IO[16]		
J2.74		AF24	netc.ETH1_RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC	netc.ETH1_RMII_TX_EN	flexio2.FLEXIO[20]	gpio4.IO[20]		
J2.76		AH20	ccmsrcgpcmix.CLKO1	netc.TMR_1588_TRIG1			flexio1.FLEXIO[26]	gpio3.IO[26]		
J2.77		L51	gpio2.IO[7]	spi3.PCS1			spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]
J2.78		AF28	netc.ETH1_RGMII_TXD[2]	INPUT=netc.ETH1_RMII_REF50_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT	sai2.RX_DATA[1]	sai4.TX_SYNC	flexio2.FLEXIO[17]	gpio4.IO[17]		
J2.79		K46	gpio2.IO[4]	tpm3.CH0	pdm.CLK	can4.TX	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]
J2.80		AF20	ccmsrcgpcmix.CLKO2	netc.TMR_1588_PP1			flexio1.FLEXIO[27]	gpio3.IO[27]		
J2.81		L45	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	can4.RX	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]
J2.83		L49	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]		spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]
J2.85		N49	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]		spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]

Pin	Assembly	Ball	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J2.86		N45	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	flexio1.FLEXIO[12]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC
J2.87		P44	gpio2.IO[15]	uart3.RX			spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]
J2.88		E49	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]		
J2.89		N51	gpio2.IO[14]	uart3.TX			spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]
J2.90		F52	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]		

Table 7: DART-MX95_J3 PINMUX

Pin	Assembly	Ball	Alt0	Alt1	Alt2	Alt3	Alt4	Alt5	Alt6	Alt7
J3.01		M44	gpio2.IO[8]	spi3.PCS0			tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]
J3.03		M46	gpio2.IO[9]	spi3.SIN			tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]
J3.28		T44	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	can5.TX	tpm5.CH1	tpm6.EXTCLK	i2c5.SDA	flexio1.FLEXIO[22]
J3.36		T46	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	can5.RX	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]
J3.38		V52	gpio5.IO[12]	pcie1.CLKREQ_B	uart6.TX		spi4.PCS2			
J3.42		V46	gpio2.IO[30]	i2c4.SDA	can5.TX					flexio1.FLEXIO[30]
J3.46		V48	gpio2.IO[31]	i2c4.SCL	can5.RX					flexio1.FLEXIO[31]
J3.48		W45	gpio5.IO[13]		uart6.RX		spi4.PCS1			
J3.50		F48	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]		
J3.52		W49	gpio5.IO[14]		uart6.CTS_B		spi4.PCS0			
J3.54		T48	gpio2.IO[24]	usdhc3.DATA0			tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]
J3.58		W51	gpio5.IO[15]	pcie2.CLKREQ_B	uart6.RTS_B		spi4.SIN			
J3.62		Y52	gpio5.IO[17]		uart7.RX		spi4.SCK			
J3.64		T52	gpio2.IO[25]	usdhc3.DATA1	can2.TX		tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]

8. SOM's interfaces

Acronym used in the tables listed under this section:

Table 8: Interface Tables Mnemonics

Column Heading		Meaning
PIN#	**Jx.YY**	Pin number on a connector: Jx: Can be J1 J2 or J3 YY: Can be 1 to 90
ALT NAME		Pin type & direction
ALT#		Alternate number for the function. Blank in case the function origin is a PHY pin.
NOTES		This column displays any special note related to the specific pin with the specific ASSY.
BALL	**XX.YY**	Source device and its pin number; See Table 2.

Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 9: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe, ETH 10G TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including Ethernet, PCIe clocks, ETH 10G clock, MIPI (CSI and DSI), LVDS lines	100 Ω Differential

8.1 Display Interfaces

The DART-MX95 supports all display interfaces MIPI DSI and LVDS display interfaces available by the i.MX 95 SoC.

The i.MX 95 SoC has the following display controllers

- 2x 4-lane or 1x 8-lane LVDS
- 1x MIPI-DSI 4-lane (w/PHY) (muxed with 1x CSI)

Which can support:

- Up to 1080p60 LVDS Tx (2x 4-lane or 1x 8-lane)
- 1x 350 MHz MIPI-DSI (4-lane, 2.5 Gbps/lane) supporting 4kp30 or 3840 x 1440p60

8.1.1 LVDS

There are 2 LVDS channels. The output of each is used to communicate RGB data and control external LCD displays.
The LVDS ports may be used as follows:

- Single channel output
- Dual channel output (one input source, two channels outputs for two displays)
- Split channel output (one input source, split to 2 channels on output)
- Separate 2 channel output

The output LVDS port complies to the below standards:

- ANSI EIA-644-A. Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.
- SPWG Notebook Panel Specification (V3.8 from 03/2007)
- PSWG standards (Panel Standardization Working Group) - set of standards for panels using LVDS.
- DISM Standard JEIDA-59-1999

8.1.1.1 LVDS0 Signals

Table 10: LVDS0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
J3.13		LVDS0_CLK_N		Differential Pair Negative side	A5
J3.11		LVDS0_CLK_P		Differential Pair Positive side	B4
J3.04		LVDS0_D0_N		Differential Pair Negative side	G9
J3.02		LVDS0_D0_P		Differential Pair Positive side	G7
J3.08		LVDS0_D1_N		Differential Pair Negative side	F8
J3.06		LVDS0_D1_P		Differential Pair Positive side	F6
J3.07		LVDS0_D2_N		Differential Pair Negative side	E7
J3.05		LVDS0_D2_P		Differential Pair Positive side	D6
J3.19		LVDS0_D3_N		Differential Pair Negative side	E9
J3.17		LVDS0_D3_P		Differential Pair Positive side	D8

8.1.1.2 LVDS1 Signals

Table 11: LVDS1 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.25	no DSCM	LVDS1_CLK_N		Differential Pair Negative side	D4
J3.23	no DSCM	LVDS1_CLK_P		Differential Pair Positive side	D2
J3.14	no DSCM	LVDS1_D0_N		Differential Pair Negative side	A3
J3.12	no DSCM	LVDS1_D0_P		Differential Pair Positive side	B2
J3.18	no DSCM	LVDS1_D1_N		Differential Pair Negative side	C3
J3.16	no DSCM	LVDS1_D1_P		Differential Pair Positive side	C1
J3.29	no DSCM	LVDS1_D2_N		Differential Pair Negative side	E3
J3.31	no DSCM	LVDS1_D2_P		Differential Pair Positive side	E1
J3.22	no DSCM	LVDS1_D3_N		Differential Pair Negative side	F4
J3.20	no DSCM	LVDS1_D3_P		Differential Pair Positive side	F2

8.1.2 MIPI DSI/CSI combo

The i.MX 95 incorporates the MIPI DSI/CSI Combo Complex,
In the DSI/CSI Combo Complex, the DSI controller provides an interface that allows communication between the processor and MIPI DSI-compliant display devices and the CSI-2 controller provides an interface between the processor and CSI-2 compliant sensors. The Rx/Tx DPHY acts as the physical layer used by the DSI and CSI-2 protocols for physical and electrical communication.

NOTE

The Rx/Tx D-PHY is shared internally in the SoC between the DSI controller and the CSI-2 controller #1, therefore the CSI-RX and DSI-TX cannot be used at the same time.

The Key features of MIPI DSI controller are listed as following:

- Support one 4-lane MIPI DSI display with pixels from the display controller
- Compliant to MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2
- The maximum pixel clock is 350 MHz.
- The maximum data rate per lane is 2.5 Gbps.

8.1.2.1 MIPI-DSI/CSI Signals Two Alternative Pinouts

DART-MX95 exposes the MIPI-DSI/CSI on one of two alternative pinouts:

1. By default, in ***"no DSCM"*** assembly, the MIPI-DSI/CSI balls will be exposed in the location of the MIPI_CSI#2 pins of the DART carrier board pinout. This is not compatible with DART-MX8M & DART-MX8M-MINI; With this option both LVDS channels and MIPI-DSI are exposed.
2. With "***DSCM***" configuration the MIPI-DSI/CSI is exposed instead of LVDS1 location; This will be compatible with DART-MX8M & DART-MX8M-MINI; With this option LVDS0 channel will still be exposed.

8.1.2.2 DSI/CSI Signals

Table 12: MIPI DSI/CSI Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.29	DSCM	DSICSI_CLK_N	0	Two alternative locations exist!; Differential Pair Negative side	C11
J3.70	no DSCM	DSICSI_CLK_N	0	Two alternative locations exist!; Differential Pair Negative side	C11
J3.31	DSCM	DSICSI_CLK_P	0	Two alternative locations exist!; Differential Pair Positive side	B10
J3.72	no DSCM	DSICSI_CLK_P	0	Two alternative locations exist!; Differential Pair Positive side	B10
J3.14	DSCM	DSICSI_D0_N	0	Two alternative locations exist!; Differential Pair Negative side	C15
J3.84	no DSCM	DSICSI_D0_N	0	Two alternative locations exist!; Differential Pair Negative side	C15
J3.12	DSCM	DSICSI_D0_P	0	Two alternative locations exist!; Differential Pair Positive side	B14
J3.86	no DSCM	DSICSI_D0_P	0	Two alternative locations exist!; Differential Pair Positive side	B14
J3.18	DSCM	DSICSI_D1_N	0	Two alternative locations exist!; Differential Pair Negative side	A13
J3.80	no DSCM	DSICSI_D1_N	0	Two alternative locations exist!; Differential Pair Negative side	A13
J3.16	DSCM	DSICSI_D1_P	0	Two alternative locations exist!; Differential Pair Positive side	B12
J3.82	no DSCM	DSICSI_D1_P	0	Two alternative locations exist!; Differential Pair Positive side	B12
J3.25	DSCM	DSICSI_D2_N	0	Two alternative locations exist!; Differential Pair Negative side	A9
J3.88	no DSCM	DSICSI_D2_N	0	Two alternative locations exist!; Differential Pair Negative side	A9
J3.23	DSCM	DSICSI_D2_P	0	Two alternative locations exist!; Differential Pair Positive side	B8
J3.90	no DSCM	DSICSI_D2_P	0	Two alternative locations exist!; Differential Pair Positive side	B8
J3.22	DSCM	DSICSI_D3_N	0	Two alternative locations exist!; Differential Pair Negative side	C7
J3.76	no DSCM	DSICSI_D3_N	0	Two alternative locations exist!; Differential Pair Negative side	C7
J3.20	DSCM	DSICSI_D3_P	0	Two alternative locations exist!; Differential Pair Positive side	B6
J3.78	no DSCM	DSICSI_D3_P	0	Two alternative locations exist!; Differential Pair Positive side	B6
J3.29	DSCM	DSICSI_CLK_N	0	Two alternative locations exist!; Differential Pair Negative side	C11

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.70	no DSCM	DSICSI_CLK_N	0	Two alternative locations exist!; Differential Pair Negative side	C11
J3.31	DSCM	DSICSI_CLK_P	0	Two alternative locations exist!; Differential Pair Positive side	B10

8.2 Camera Interface

8.2.1 MIPI Camera Serial Interface

The MIPI CSI-2 host controller implements the CSI-2 protocol on the host side. The CSI-2 link protocol specification is a part of communication protocols defined by MIPI Alliance standards intended for mobile system chip-to-chip communications. The CSI-2 specification is for the image application processor communication in cameras.

The MIPI CSI-2 includes the following features:

- Compliant with MIPI Alliance standards
  - MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 2.0
  - MIPI Alliance Specification for D-PHY, Version 1.2 up to 2.5 Gbps
- Supports high speed, low power, and ultra-low power state modes
- Provides raw throughput up to 10 Gbps (D-PHY 4 lanes)
- Supports up to 8 virtual channels
- Data scrambling for electromagnetic interference (EMI) mitigation
- Provides vertical and horizontal timing synchronization signals
- Primary and secondary data formats:
  - YUV420 8-bit / 10-bit / 8-bit (CSPS) / 10-bit (CSPS)
  - YUV422 8-bit / 10-bit
  - RGB888 / RGB666 / RGB565 / RGB555 / RGB444
  - RAW6 / RAW7 / RAW8 / RAW10 / RAW12 / RAW14 / RAW16 / RAW20
  - User defined byte-based data
  - Embedded data
  - Generic 8-bit long packet data types
  - Non-pixel data short packets
- Error detection and correction
  - PHY level such as synchronization pattern mismatch
  - Packet level (ECC and CRC)
  - Line level
  - Frame level
- PHY Protocol Interface (PPI) Pattern Generator for pattern injection in debugging post-validation practice of PPI

8.2.2 MIPI-CSI2 Signals

The DART-MX95 exposes the 2x MIPI-CSI2 input ports of the iMX 95 SOC.

- MIPI-CSI2 #1 (combo MIPI-CSI and DSI) is exported from the MIPI DSI/CSI combo pins and has 2 Two alternative locations see pinout table in section 8.1.2.2
- MIPI-CSI2 #0 (standalone MIPI-CSI) is exported on the pins listed below.

8.2.2.1 MIPI-CSI2 Port 0 Signals

Table 13: MIPI-CSI2 P0 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J1.89		MIPI_CSI_CLK_N		Differential Pair Negative side	F16
J1.87		MIPI_CSI_CLK_P		Differential Pair Positive side	E15
J1.83		MIPI_CSI_D0_N		Differential Pair Negative side	F20
J1.81		MIPI_CSI_D0_P		Differential Pair Positive side	E19
J1.75		MIPI_CSI_D1_N		Differential Pair Negative side	D18
J1.73		MIPI_CSI_D1_P		Differential Pair Positive side	E17
J1.77		MIPI_CSI_D2_N		Differential Pair Negative side	D14
J1.79		MIPI_CSI_D2_P		Differential Pair Positive side	E13
J1.71		MIPI_CSI_D3_N		Differential Pair Negative side	F12
J1.69		MIPI_CSI_D3_P		Differential Pair Positive side	E11

8.3 Ethernet Interface

The DART-MX95 exposes implements 3x Ethernet controllers capable of simultaneous operation.

- 2x 10/100/1000 Mbps Ethernet controllers ENET1/2 supporting: 1.8V/3.3V RMII operation, 1.8V RGMII operation, Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588. One of two Ethernet controllers support 802.1Qbu Frame Preemption. Both of Ethernet controllers support 802.1Qbv enhancements for Scheduling Traffic, Timing Specific Departure (TSD), and 802.1Qci Per-stream Filtering and Policing (PSFP).
- 1x 10 Gigabit Ethernet controller supports XFI, SGMII (2.5 G and 1G), and 10G-USXGMII (single 10GE mode only)

8.3.1 ENET1

The SOM can be ordered in one of the following configurations:

- **"EC" configuration** – The DART-MX95 includes an on SOM a Gigabit PHY (Max Linear MXL86110) connected to ENET1 RGMII interface signals. External connector and magnetics should be implemented on carrier board to complete the interface to the media.

- **"no EC" configuration** - The DART-MX95 exposes the ENET1 RGMII/RMII interface signals to the connector.
  J1.31 which is PF09 PMIC LDO1 output, provides internally the power supply for NVCC_ENET domain which sets ENET1/2 reference voltage.
  Default voltage is set to 3.3V, for ENET1/2 RGMII support, voltage should be set to 1.8V.

8.3.1.1 Ethernet PHY

The on-SOM MaxLinear MxL86110x Gigabit PHY in conjunction with external magnetics on carrier board complete the interface to the media.

Table 14: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 15: Ethernet PHY Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J1.09	EC	LED_ACT		Signal source is Ethernet PHY; In "EC" configuration - LED, Runs@3.3V	MxL86110x.34
J1.05	EC	LED_LINK10_100		Signal source is Ethernet PHY; In "EC" configuration - connected to GND	GND
J1.07	EC	LED_LINK1000		Signal source is Ethernet PHY; In "EC" configuration - LED, Runs@3.3V	MxL86110x.33
J1.06	EC	ETH_TRX0_N		Signal source is Ethernet PHY; Differential Pair Negative side	MxL86110x.2
J1.08	EC	ETH_TRX0_P		Signal source is Ethernet PHY; Differential Pair Positive side	MxL86110x.1
J1.04	EC	ETH_TRX1_N		Signal source is Ethernet PHY; Differential Pair Negative side	MxL86110x.5
J1.02	EC	ETH_TRX1_P		Signal source is Ethernet PHY; Differential Pair Positive side	MxL86110x.4
J1.12	EC	ETH_TRX2_N		Signal source is Ethernet PHY; Differential Pair Negative side	MxL86110x.7
J1.10	EC	ETH_TRX2_P		Signal source is Ethernet PHY; Differential Pair Positive side	MxL86110x.6
J1.16	EC	ETH_TRX3_N		Signal source is Ethernet PHY; Differential Pair Negative side	MxL86110x.10
J1.14	EC	ETH_TRX3_P		Signal source is Ethernet PHY; Differential Pair Positive side	MxL86110x.9

Table 16: MxL86110x Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	OFF	OFF	OFF	OFF
LED_LINK_1000	ON	ON	ON	ON	ON	ON
LED_ACT	OFF	BLINK	OFF	BLINK	OFF	BLINK
ON = active; OFF = inactive						

8.3.1.2 ENET1 Signals

Table 17: ENET1 Signals

PIN#	ASSY	ALTNAME	ALT#	NOTES	BALL
J1.06	no EC	INPUT=netc.ETH0_RMII_REF50_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AF36
J1.07	no EC	netc.ETH0_RGMII_RX_CLK	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface; ENET RGMII Receive Clock: 125MHz @ 1000Mbps /	AJ33

PIN#	ASSY	ALTNAME	ALT#	NOTES	BALL
				25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	
J1.09	no EC	netc.ETH0_RGMII_RX_CTL	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Receive data Control	AH34
J1.10	no EC	netc.ETH0_RGMII_RXD[0]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ35
J1.12	no EC	netc.ETH0_RGMII_RXD[1]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AK36
J1.14	no EC	netc.ETH0_RGMII_RXD[2]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ37
J1.16	no EC	netc.ETH0_RGMII_RXD[3]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AH38
J1.05	no EC	netc.ETH0_RGMII_TX_CLK	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface; ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	AG31
J1.03	no EC	netc.ETH0_RGMII_TX_CTL	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Transmit data Control	AF32
J1.04	no EC	netc.ETH0_RGMII_TXD[0]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG33
J1.02	no EC	netc.ETH0_RGMII_TXD[1]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG35
J1.06	no EC	netc.ETH0_RGMII_TXD[2]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AF36
J1.08	no EC	netc.ETH0_RGMII_TXD[3]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG37
J1.09	no EC	netc.ETH0_RMII_CRS_DV	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Receive data Control	AH34
J1.07	no EC	netc.ETH0_RMII_RX_ER	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface; ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	AJ33
J1.14	no EC	netc.ETH0_RMII_RX_ER	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ37

PIN#	ASSY	ALTNAME	ALT#	NOTES	BALL
J1.10	no EC	netc.ETH0_RMII_RXD[0]	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ35
J1.12	no EC	netc.ETH0_RMII_RXD[1]	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AK36
J1.03	no EC	netc.ETH0_RMII_TX_EN	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Transmit data Control	AF32
J1.04	no EC	netc.ETH0_RMII_TXD[0]	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG33
J1.02	no EC	netc.ETH0_RMII_TXD[1]	7	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG35
J1.06	no EC		1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AF36
J1.07	no EC	netc.ETH0_RGMII_RX_CLK	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface; ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	AJ33
J1.09	no EC	netc.ETH0_RGMII_RX_CTL	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Receive data Control	AH34
J1.10	no EC	netc.ETH0_RGMII_RXD[0]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ35
J1.12	no EC	netc.ETH0_RGMII_RXD[1]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AK36
J1.14	no EC	netc.ETH0_RGMII_RXD[2]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ37
J1.16	no EC	netc.ETH0_RGMII_RXD[3]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AH38
J1.05	no EC	netc.ETH0_RGMII_TX_CLK	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface; ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	AG31
J1.03	no EC	netc.ETH0_RGMII_TX_CTL	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Transmit data Control	AF32
J1.04	no EC	netc.ETH0_RGMII_TXD[0]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG33

PIN#	ASSY	ALTNAME	ALT#	NOTES	BALL
J1.02	no EC	netc.ETH0_RGMII_TXD[1]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG35
J1.06	no EC	netc.ETH0_RGMII_TXD[2]	0	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AF36

8.3.2 ENET2

ENET1 RGMII/RMII interface signals are always exported.
Signals, in conjunction with MDIO signals exported from connectors, can be used to interface an external Ethernet PHY or ethernet switch.

NOTE

ENET2 signals signal levels
"EC" configuration – referenced to 1.8V
"no EC" configuration – referenced to J1.31 level

Table 18: ENET2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.78		INPUT=netc.ETH1_RMII_REF50_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); Internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise. This sets boot source. ; RGMII Data out; As boot, control with POR_B rise: Low - Internal Boot (SD1 eMMC); High - External Boot (SD2)	AF28
J2.72		netc.ETH1_RGMII_RX_CLK	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	AJ25
J2.64		netc.ETH1_RGMII_RX_CTL	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); RGMII Receive data Control	AH26
J2.65		netc.ETH1_RGMII_RXD[0]	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ27
J2.69		netc.ETH1_RGMII_RXD[1]	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AK28
J2.66		netc.ETH1_RGMII_RXD[2]	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ29
J2.68		netc.ETH1_RGMII_RXD[3]	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31	AH30

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				(1.8V/3.3V); RGMII Data in	
J2.71		netc.ETH1_RGMII_TX_CLK	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	AG23
J2.74		netc.ETH1_RGMII_TX_CTL	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); RGMII Transmit data Control	AF24
J2.70		netc.ETH1_RGMII_TXD[0]	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG25
J2.67		netc.ETH1_RGMII_TXD[1]	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); RGMII Data out	AG27

8.3.3 MDIO, ETH control Signals

Table 19: MDIO, Power, 1588, Control & Clock Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.11		netc.MDIO	0	Runs @ 3.3V level via NTS0104GU12 level translator; Do not alter pinmux with "EC" configuration	AJ39
J2.62		netc.MDIO	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ31
J1.13		netc.MDC	0	Runs @ 3.3V level via NTS0104GU12 level translator; Do not alter pinmux with "EC" configuration	AK40
J2.63		netc.MDC	0	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK32
J1.31		ETH_3V3	0	PF09 PMIC LDO1 output; In "EC" configuration - Ethernet PHY 3.3V power supply In "no EC" configuration - NVCC_ENET domain power supply setting ENET1/2 reference voltage: Default - 3.3V, should be set to 1.8V for ENET1/2 RGMII support Max. 200mA draw allowed;	PF09.53
J2.82	EC	ETH_INT_1V8	0	Signal source is Ethernet PHY; Available in "EC" configuration; Runs @ 1.8V	MxL86110x.31
J1.84		netc.TMR_1588_ALARM1	3	Will change level according to J1.90 VDD_SDIO2;	AA49
J2.07		netc.TMR_1588_ALARM1	2	Runs @ 1.8V	AK24
J2.09		netc.TMR_1588_ALARM2	2	Runs @ 1.8V	AJ23
J1.80		netc.TMR_1588_CLK	1	Will change level according to J1.90 VDD_SDIO2;	AC49
J1.28		netc.TMR_1588_GCLK	3	Recommend using SD2_RESET_B for external SD card power cycle. Will change level according to J1.90 VDD_SDIO2;	AD52

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.82		netc.TMR_1588_PP1	1	Will change level according to J1.90 VDD_SDIO2;	AB48
J2.80		netc.TMR_1588_PP1	1	Runs @ 1.8V	AF20
J1.86		netc.TMR_1588_PP2	1	Will change level according to J1.90 VDD_SDIO2;	AC51
J1.78		netc.TMR_1588_PP3	1	Will change level according to J1.90 VDD_SDIO2;	AA51
J1.74		netc.TMR_1588_TRIG1	1	External SD card detect input; Add 10K external pull up to J1.90; Will change level according to J1.90 VDD_SDIO2;	AD48
J2.76		netc.TMR_1588_TRIG1	1	Runs @ 1.8V	AH20

8.3.4 10Gb Ethernet

The DART-MX95 exposes the i.MX95 SOC 10 Gigabit Ethernet signals required for supporting XFI, SGMII (2.5 G and 1G), and 10 G-USXGMII (single 10GE mode only). The 10Gb Ethernet port requires supplying an external 156.25MHz PCIe compliant reference clock if the function is enabled.

Table 20: 10Gb Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.35		ETH_CLKIN_N		Need to supply 156.25 MHz for 10G ETH clock reference; Differential Pair Negative side	AF14
J1.37		ETH_CLKIN_P		Need to supply 156.25 MHz for 10G ETH clock reference; Differential Pair Positive side	AG15
J1.43		ETH_RX0_N		Differential Pair Negative side	AK12
J1.45		ETH_RX0_P		Differential Pair Positive side	AJ13
J1.42		ETH_TX0_N		Differential Pair Negative side	AK16
J1.44		ETH_TX0_P		Differential Pair Positive side	AJ17

8.4 Wi-Fi, BT, 802.15.4

The DART-MX95 contains a certified high-performance Wi-Fi, Bluetooth, 802.15.4 module:

- Wi-Fi® 802.11a/b/g/n/ac/ax
- Bluetooth® 5.4 BR/EDR/LE
- 802.15.4
- Modules have an antenna connection through a 50Ω U. FL JACK connector

Figure 3 illustrates the DART-MX95 internal Wi-Fi and BT connectivity.

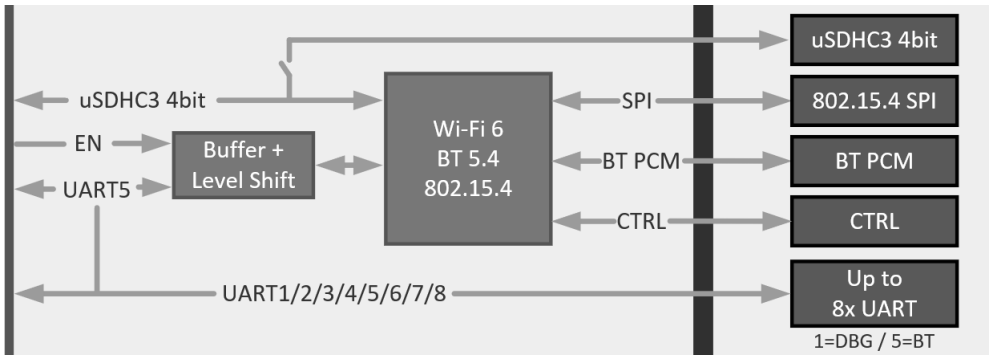


Figure 3: DART-MX95 Wi-Fi & BT Internal Connection

To allow the most flexible solution the following elements are added to the DART-MX95:

- Tristate buffer on the BT link based on UART interface.
  Will allow isolation from the Wi-Fi module and the use by external circuity via the DART-MX95 connector.
- Bluetooth PCM and special control signals can be exported in special assembly configuration.
- Dedicated uSDHC3 channel for the Wi-Fi module interface. In case no Wi-Fi module assembled, uSDHC3 can be exported to DART-MX95 connector via special assembly option.

8.4.1 Interface Implementation Options

8.4.1.1 Module Configuration with "WBD" Option

- System use: **Wi-Fi and Bluetooth**.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT module (using GPIO4_IO28)
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT module (using GPIO4_IO28).

8.4.1.2 Module Configuration with "WBE" Option

- System use: **Wi-Fi and Bluetooth and 802.15.4**.
  - BT UART external interface pins should be left floating.
  - WBE SPI pins should be connected externally to SPI I/F running at 1.8V levels.
- System use: **Wi-Fi and no BT no 802.15.4**.
  - In this case, disable the BT and 802.15.4 module (using GPIO4_IO28).
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and 802.15.4 and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT and 802.15.4 module (using GPIO4_IO28).
  - WBE SPI pins should be connected externally to SPI I/F running at 1.8V.

8.4.1.3 Module Configuration without "WBD" or "WBE" Option

- System use: **no Wi-Fi and no BT**.
  - BT UART interface accessible externally with any of its alternative functions.
  - uSDHC3 interface can be exported externally with "SDEX" assembly option. uSDHC3 is working at 1.8V levels.

8.4.2 Bluetooth Interface signals

Table 21: BT LPUART interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.20		uart5.TX	0	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J49
J2.22		uart5.RTS_B	0	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K52
J2.24		uart5.RX	0	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J51
J2.26		uart5.CTS_B	0	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K48

8.4.3 Bluetooth PCM Interface signals

Table 22: BT PCM interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.36	BTPCM	BT_PCM_IN_1V8		Signal source is WIFI module. Available in "BTPCM" configuration; Runs @ 1.8V	LBES5PL2xL.60
J1.54	BTPCM	BT_PCM_CLK_1V8		Signal source is WIFI module. Available in "BTPCM" configuration; Runs @ 1.8V	LBES5PL2xL.57
J1.56	BTPCM	BT_PCM_OUT_1V8		Signal source is WIFI module. Available in "BTPCM" configuration; Runs @ 1.8V	LBES5PL2xL.59
J1.65	BTPCM	BT_PCM_SYNC_1V8		Signal source is WIFI module. Available in "BTPCM" configuration; Runs @ 1.8V	LBES5PL2xL.61

NOTE

[1] This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

8.4.4 WBE interface signals

Table 23: WBE SPI interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.67	WBE	SPI_CLK_1V8		Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V	LBES5PL2xL.8
J1.55	WBE	SPI_CS0_1V8		Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V	LBES5PL2xL.4
J3.32	WBE	SPI_INT_1V8		Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V	LBES5PL2xL.5
J1.61	WBE	SPI_RXD_1V8		Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V	LBES5PL2xL.6
J1.41	WBE	SPI_TXD_1V8		Signal source is WIFI module. Available in "WBE" configuration; Runs @ 1.8V	LBES5PL2xL.7
J1.63	WBE& SPICM	SPI_TXD_1V8		Signal source is WIFI module. In "WBE and SPICM" configuration; Runs @ 1.8V	LBES5PL2xL.7

8.4.5 Host Wake Interface signals

The SOM exposes the WIFI/BT module wake signals.

The user is required to connect the relevant host/device wake signal to a 1.8V GPIO according to the requirements if applicable.

Table 24: WLAN/BT Host Wake

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.23	WBD/WBE	BT_HOST_WAKE_1V8		Signal source is WIFI module. Available in "WBD" or "WBE" configuration Output from WIFI module; Runs @ 1.8V	LBES5PL2xL.76
J1.25	WBD/WBE	WIFI_HOST_WAKE_1V8		Signal source is WIFI module. Available in "WBD" or "WBE" configuration Output from WIFI module; Runs @ 1.8V	LBES5PL2xL.73
J2.52	WBD/WBE	BT_DEV_WAKE_1V8		Signal source is WIFI module. Available in "WBD" or "WBE" configuration Input to WIFI module; Runs @ 1.8V	LBES5PL2xL.75

8.4.6 WIFI control signals

Table 25: WIFI control interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.64	RFCTRL	RF_CNTL0_1V8		Signal source is WIFI module. Available in "RFCTRL" configuration; Runs @ 1.8V	LBES5PL2xL.27
J1.39	RFCTRL	RF_CNTL1_1V8		Signal source is WIFI module. Available in "RFCTRL" configuration; Runs @ 1.8V	LBES5PL2xL.26
J1.66	RFCTRL	RF_CNTL3_1V8		Signal source is WIFI module. Available in "RFCTRL" configuration; Runs @ 1.8V	LBES5PL2xL.25
J1.68	RFCTRL	RF_CNTL4_1V8		Signal source is WIFI module. Available in "RFCTRL" configuration; Runs @ 1.8V	LBES5PL2xL.24
J1.52	BTRST	BT_KILL_1V8		Signal source is WIFI module. Available in "BTRST" configuration; Runs @ 1.8V	LBES5PL2xL.64
J1.70	BTRST	LR_KILL_1V8		Signal source is WIFI module. Available in "BTRST" configuration; Runs @ 1.8V	LBES5PL2xL.38
J1.58	WRST	WB_KILL_1V8		Signal source is WIFI module. Available in "WRST" configuration; Runs @ 1.8V	LBES5PL2xL.63
J2.37	COEX	COEX_SIN_1V8		Signal source is WIFI module. Available in "COEX" configuration; Runs @ 1.8V	LBES5PL2xL.69
J2.39	COEX	COEX_SOUT_1V8		Signal source is WIFI module. Available in "COEX" configuration; Runs @ 1.8V	LBES5PL2xL.70

NOTE

[1] This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

8.5 MMC/SD/SDIO

The DART-MX95 exposes uSDHC2/3 interfaces of the iMX 95 SOC.
The following tables list the interface pinout for SD2/3 signals.

The exposed uSDHC controllers can support up to a 4-bit interface designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.0.
- 1.8 V and 3.3 V operation. Does not support 1.2 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

8.5.1 SD1 signals

The uSDHC1 controller (SD1) is used internally for the eMMC.

8.5.2 SD2 signals

Table 26: uSDHC2 interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.74		usdhc2.CD_B	0	External SD card detect input; Add 10K external pull up to J1.90; Will change level according to J1.90 VDD_SDIO2;	AD48
J1.82		usdhc2.CLK	0	Will change level according to J1.90 VDD_SDIO2;	AB48
J1.88		usdhc2.CMD	0	Will change level according to J1.90 VDD_SDIO2;	AB52
J1.86		usdhc2.DATA0	0	Will change level according to J1.90 VDD_SDIO2;	AC51
J1.80		usdhc2.DATA1	0	Will change level according to J1.90 VDD_SDIO2;	AC49
J1.78		usdhc2.DATA2	0	Will change level according to J1.90 VDD_SDIO2;	AA51
J1.84		usdhc2.DATA3	0	Will change level according to J1.90 VDD_SDIO2;	AA49
J1.28		usdhc2.RESET_B	0	Recommend using SD2_RESET_B for external SD card power cycle. Will change level according to J1.90 VDD_SDIO2;	AD52
J1.90		VDD_SDIO2	0	Power output for SD2 pins reference 1.8V/3.3V- set by DART PMIC;	PF09.3

8.5.3 SD3 signals

The uSDHC3 controller is used internally for the Wi-Fi interface on the SOM.
It can be used externally when the Wi-Fi is not assembled in a SOM with “SDEX” assembly.

Table 27: uSDHC3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.45	SDEX	usdhc3.CLK	0	Available in "SDEX" configuration; Runs @ 1.8V	AG51
J2.60		usdhc3.CLK	1	Duplicate pin on J3.28	T44
J3.28		usdhc3.CLK	1	Duplicate pin on J2.60	T44
J2.43	SDEX	usdhc3.CMD	0	Available in "SDEX" configuration; Runs @ 1.8V	AF48
J2.54		usdhc3.CMD	1	Duplicate pin on J3.36	T46
J3.36		usdhc3.CMD	1	Duplicate pin on J2.54	T46
J2.35	SDEX	usdhc3.DATA0	0	Available in "SDEX" configuration; Runs @ 1.8V	AG49
J3.54		usdhc3.DATA0	1		T48
J2.33	SDEX	usdhc3.DATA1	0	Available in "SDEX" configuration; Runs @ 1.8V	AH52
J3.64		usdhc3.DATA1	1		T52
J2.10	no AC	usdhc3.DATA2	1		U45
J2.31	SDEX	usdhc3.DATA2	0	Available in "SDEX" configuration; Runs @ 1.8V	AE49
J2.29	SDEX	usdhc3.DATA3	0	Available in "SDEX" configuration; Runs @ 1.8V	AF52

8.6 USB Ports

The DART-MX95 supports two USB controllers and PHYs.

- **USB1** – USB 3.0 Type C with PHY. This USB Controller and PHY supports either USB 2.0 or USB 3.0 operation, including USB Type C's ability to support two sets of USB Superspeed SerDes lanes, with data potentially received or transmitted on either lane.

  The USB Type C PHY incorporates a "Type-C Assist Block", which identifies which of the two Superspeed lanes are to be used at any given time.

  Note: In default Variscite BSP Release the SS identification mechanism is disabled therefore requiring connection of only 1x USB3 SS RX/TX pair. If required, this mechanism can be enabled in SW.

  The port can be used as USB Host or USB Device.

- **USB2 -** USB 2.0 Type with PHY. This USB Controller and PHY supports USB 2.0 operation.

  The port can be used as USB Host or USB Device.

NOTE

The document uses the term "OTG" throughout. USB core hardware does not support the automatic OTG function by hardware. It is a dual-role (Host and Device mode) core, which you can implement in software with the hardware assist.

USB3 PHY

USB3_PHY provides the following general features:

- Type-C support for flexibility with cable reversal and plug flip
- Built-in VBus threshold comparators
- Single reference clock input for both USB 3.0 and USB 2.0 operating modes
- Integrated 3.3-V-to-1.8-V regulator in the PHY

USB3_PHY provides the following USB 3.0 features:

- 5 Gbit/s SuperSpeed data transmission rate through 3 m USB 3.0 cable
- PIPE 3-compliant SuperSpeed USB 3.0 transceiver interface
- Integrated PHY includes transmitter, receiver, SSC generation, PLL, digital core, and ESD
- Adaptive Rx equalization
- Low-jitter PLL technology with excellent supply isolation

USB3_PHY provides the following USB 2.0 features:

- Built-in VBus threshold comparators

- 480 Mbit/s high-speed, 12 Mbit/s full-speed, and 1.5 Mbit/s low-speed serial (host mode only) data transmission rates
- Supports high-speed power modes: suspend, resume, and remote wakeup
- 45 Ω termination, 1.5 kΩ pullup and 15 kΩ pulldown resistors with support for independence control of the pull-down resistors
- 8/16-bit unidirectional parallel interfaces for HS, FS, and LS (host mode only) modes of operation in accordance with the UTMI+ specification
- Dual (HS/FS) mode host/device support
- Data recovery from serial data on the USB connector
- SYNC/end-of-packet (EOP) generation and checking
- Bit stuffing and unstuffing, and bit-stuffing error detection
- Non return to zero invert (NRZI) encoding and decoding
- Bit serialization and deserialization
- VBus threshold comparators

USB2 PHY

USB 2.0 PHY provides the following general features:

- Implements low power dissipation while active, idle, or on standby
- Fully integrates high-, full-, and low-speed (Host mode only) termination and signal switching
- Implements one parallel data interface and clock for high-, full-, and low-speed (Host mode only) USB data transfers
- Provides on-chip PLL to reduce clock noise and eliminate the need for an external clock generator
- Provides Universal Asynchronous Receiver/Transmitter (UART) support to enable the USB 2.0 PHY to receive and transmit asynchronous, serial data

USB 2.0 PHY provides the following USB 2.0 features:

- Supports 480-Mbps high-speed, 12-Mbps full-speed, and 1.5-Mbps low-speed (Host mode only) data transmission rates
- Supports 8/16-bit unidirectional parallel interfaces for HS, FS, and LS (Host mode only) modes of operation, in accordance with the UTMI+ specification
- Provides dual (HS/FS) mode host support
- Implements data recovery from serial data on the USB connector
- Implements SYNC/End-of-Packet (EOP) generation and checking
- Implements Non Return to Zero Invert (NRZI) encoding and decoding Implements logic to support suspend, sleep, resume, and remote wakeup operations
- Supports battery charging to enable devices to draw current in excess of the USB 2.0 specification for charging and/or powering up from dedicated charging ports or charging downstream ports

8.6.1 USB Port1 interface signals

Table 28: USB3.0/2.0 Port 1 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.67		USB1_DN		USB OTG signal	B18
J3.65		USB1_DP		USB OTG signal	C19
J3.56		USB1_ID		USB1 PHY native ID analog input; No GPIO function; Usage not recommended; NXP recommends using any GPIO to implement OTG function.	C23
J3.53		USB1_RX0_N		Differential Pair Negative side	B20
J3.55		USB1_RX0_P		Differential Pair Positive side	A21
J3.35		USB1_RX1_N		Differential Pair Negative side	A17
J3.37		USB1_RX1_P		Differential Pair Positive side	B16
J3.59		USB1_TX0_N		Differential Pair Negative side	E25
J3.61		USB1_TX0_P		Differential Pair Positive side	D26
J3.41		USB1_TX1_N		Differential Pair Negative side	D22
J3.43		USB1_TX1_P		Differential Pair Positive side	E21
J3.66		USB1_VBUS		5V tolerant; VBUS detect input	E23

8.6.2 USB Port2 interface signals

Table 29: USB2.0 Port 2 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.49		USB2_DN		USB OTG signal	A25
J3.47		USB2_DP		USB OTG signal	B24
J3.44		USB2_ID		USB2 PHY native ID analog input; No GPIO function; Usage not recommended; NXP recommends using any GPIO to implement OTG function.	F24
J3.26		USB2_VBUS		5V tolerant; VBUS detect input	E27

8.6.3 USB interface signals

The Table below lists the available DART-MX95 exposed pins, which can be optionally used to implement a complete USB functionality.

Table 30: USB Port 1 & 2 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.02	no EC	usb1.OTG_OC	3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG35
J1.11		usb1.OTG_PWR	3	Runs @ 3.3V level via NTS0104GU12 level translator	AJ39
J1.08	no EC	usb2.OTG_ID	3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG37
J1.06	no EC	usb2.OTG_OC	3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AF36
J1.09	no EC	usb2.OTG_PWR	3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AH34

8.7 PCIe

DART-MX95 PCI exposes two PCI Express GEN 3.0 single lane interfaces. The PCI Express ports require an external 100MHz PCIe compliant reference clock if the function is enabled.

The PCIe controller supports:

- All non-optional features of the PCI Express Base Specification, Revision 5.0, Version 1.0
- Optional features of the specification, which include:
  - Completion Timeout Ranges
  - L1 Substates (L1SS)
  - Separate Refclk with Independent Spread Spectrum Clocking (SRIS)
  - Gen3 Receiver Impedance
  - PCI Express Active State Power Management (ASPM)
  - PCI Express Advanced Error Reporting (AER) with Multiple Header Logging
- Up to x1 Gen1, Gen2, Gen3
- Internal Address Translation Unit (iATU)
- ACE-Lite bridge
- Embedded DMA with Hardware Flow Control:
  - Four channels for reading
  - Four channels for writing
- One Virtual Channel (VC0)
- Store-and-forward Queue Modes for Rx TLPs
- 256 bytes of Max Payload Size (MAX_PAYLOAD_SIZE)
- Configurable BAR Filtering, I/O Filtering, Configuration Filtering and Completion Lookup/Timeout
- MSI with Per-Vector Masking (PVM), Extended message data for MSI
- Root Complex (RC) and End Point (EP) Configurations
- Transaction Filtering and Routing Look up

8.7.1 PCIE1 Signals

Table 31: PCIE1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.51		PCIE1_CLKIN_N		Need to supply 100MHz PCIe clock reference; Differential Pair Negative side	C31
J1.53		PCIE1_CLKIN_P		Need to supply 100MHz PCIe clock reference; Differential Pair Positive side	B30
J1.60		PCIE1_RX0_N		Differential Pair Negative side	A29
J1.62		PCIE1_RX0_P		Differential Pair Positive side	B28
J1.57		PCIE1_TX0_N		Differential Pair Negative side	D30
J1.59		PCIE1_TX0_P		Differential Pair Positive side	E29

8.7.2 PCIE1 Side band signals

Table 32: PCIE1 Side band signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.38		pcie1.CLKREQ_B	1		V52

8.7.3 PCIE2 Signals

Table 33: PCIE2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.54	no SPICM & no BTPCM & no RFCTRL	PCIE2_CLKIN_N		In "no SPICM" and "no BTPCM " and "no RFCTRL" configuration - Need to supply 100MHz PCIe clock reference; Differential Pair Negative side	A33
J1.56	no SPICM & no BTPCM & no RFCTRL	PCIE2_CLKIN_P		In "no SPICM" and "no BTPCM " and "no RFCTRL" configuration - Need to supply 100MHz PCIe clock reference; Differential Pair Positive side	B32
J1.63	no SPICM & no BTPCM & no RFCTRL	PCIE2_RX0_N		Differential Pair Negative side	C35
J1.65	no SPICM & no BTPCM & no RFCTRL	PCIE2_RX0_P		Differential Pair Positive side	B34
J1.66	no SPICM & no BTPCM & no RFCTRL	PCIE2_TX0_N		Differential Pair Negative side	F32
J1.68	no SPICM & no BTPCM & no RFCTRL	PCIE2_TX0_P		Differential Pair Positive side	E31

8.7.4 PCIE2 Side band signals

Table 34: PCIE2 Side band signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.58		pcie2.CLKREQ_B	1		W51

8.8 Audio

The DART-MX95 features analog and digital type of audio interfaces:

- WM8904 Audio codec Analog outputs & input interfaces:
  - Stereo line input
  - Stereo HP output
  - Digital microphone input
- **S**ynchronous **A**udio **I**nterface (SAI)
- **S**ony **P**hilips **D**igital **I**nter**F**ace (SPDIF)
- **P**ulse **D**ensity **M**odulation (PDM)
- **M**edium **Q**uality **S**ound (MQS)
- Audio transceiver differential pair (AUD)

8.8.1 Analog Audio

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

Figure 4 illustrates the connectivity for no large AC coupling capacitors

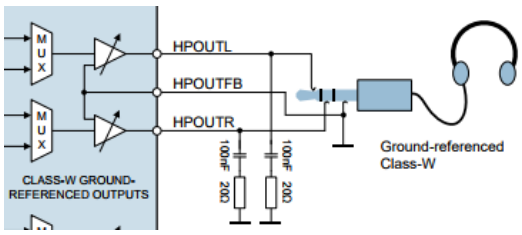


Figure 4: WM8904 Headphone connectivity

Refer to the official data sheet for detailed electrical characteristics of the relevant interfaces.

8.8.1.1 Analog Audio Signals

Table 35: Analog Audio Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.02	AC	HPLOUT		Signal source is Audio Codec; Left headphone output (line or headphone output); 100nF and 20Ω Zobel network required	WM8904.13
J2.04	AC	HPROUT		Signal source is Audio Codec; Right headphone output (line or headphone output); 100nF and 20Ω Zobel network required	WM8904.15
J2.06	AC	HPOUTFB		Signal source is Audio Codec; Headphone output ground loop noise rejection feedback;	WM8904.14

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.08	AC	LINEIN1_LP		Signal source is Audio Codec; Left channel input;	WM8904.26
J2.10	AC	LINEIN1_RP		Signal source is Audio Codec; Right channel input;	WM8904.24
J2.12		AGND		Connect to GND;	AGND
J2.14	AC	DMIC_CLK		Signal source is Audio Codec; DMIC output 3.3V level;	WM8904.01
J2.16	AC	DMIC_DATA		Signal source is Audio Codec; DMIC input is 1.8V level; Add ~500 Ohm voltage divider;	WM8904.27

8.8.2 SAI - Synchronous Audio Interface

The SAI module of the iMX 95 SOC provides an interface that supports full-duplex serial digital audio interfaces with frame synchronization formats such as I2S, AC97, TDM, and Codec/DSP interfaces.

SAI includes the following Features:

- Transmitter with independent bit clock and frame synchronization supporting 2 data lines
- Receiver with independent bit clock and frame synchronization supporting 2 data lines
- Maximum frame size of 32 words per data line
- Word length of 8 to 32 bits
- Word length configured separately for the first word and remaining words in a frame
- Asynchronous 32 × 32-bit FIFO for each transmit and receive data line supports:
    - Graceful restart after FIFO error.
    - Automatic restart after FIFO error without software intervention.
    - 8-bit and 16-bit data packing into each 32-bit FIFO word.
    - Multiple-data-line FIFOs combining into single-data-line FIFO.
- Independent 32-bit timestamp counters and bit counters for monitoring transmit and receive progress

NOTE

Some of the features can vary among chips and among SAI modules on the same chip. See i.MX 95 Applications Processors Reference Manual for further details.

SAI1 is in AON domain, SAI2 in NETC domain, SAI3-SAI5 in Wakeup domain.

8.8.2.1 SAI Signals Definitions

The following table details the SAI interface signals definition.

Table 36: SAI interface signals definition

NAME	FUNCTION	DIR
TX_BCLK	Transmit bit clock: the bit clock is an input when externally generated and an output when internally generated.	I/O
TX_SYNC	Transmit frame sync: the frame sync is an input sampled synchronously by the bit clock when externally generated. It is an output generated synchronously by the bit clock when internally generated.	I/O
TX_DATA[1:0]	Transmit data: the bit clock synchronously generates the transmit data; this signal is 3-stated when not transmitting a word.	O
RX_BCLK	Receive bit clock: the bit clock is an input when externally generated and an output when internally generated.	I/O
RX_SYNC	Receive frame sync: the frame sync is an input sampled synchronously by the bit clock when externally generated. It is an output generated synchronously by the bit clock when internally generated.	I/O
RX_DATA[1:0]	Receive data: the bit clock synchronously samples the receive data.	I
MCLK	Audio controller clock: the audio controller clock is an input when externally generated and an output when internally generated.	I/O

8.8.2.2 SAI1 Signals

Table 37: SAI1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.36		sai1.MCLK	1		H52
J2.46		sai1.MCLK	4		E51
J2.40		sai1.RX_BCLK	4		E45
J2.36		sai1.RX_DATA[0]	0		H52
J2.34		sai1.RX_SYNC	4		E43
J2.38		sai1.TX_BCLK	0		G51
J1.72		sai1.TX_DATA[0]	0	Duplicate pin on J2.44 BOOT_MODE3 pin, Has internal 10K PU to J1.27 (3.3V); Do not drive until after POR_B rise + 30ms; GPIO can be output only or tristated.	H48
J2.44		sai1.TX_DATA[0]	0	Duplicate pin on J1.72; see J1.72 note	H48
J2.13		sai1.TX_DATA[1]	1	Duplicate pin on J2.42 BOOT_MODE2 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull down; GPIO can be output only or tristated.	G49
J2.42		sai1.TX_DATA[1]	1	Duplicate pin on J2.13; see J2.13 note	G49
J2.13		sai1.TX_SYNC	0	Duplicate pin on J2.42 BOOT_MODE2 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull down; GPIO can be output only or tristated.	G49
J2.42		sai1.TX_SYNC	0	Duplicate pin on J2.13; see J2.13 note	G49

8.8.2.3 SAI2 Signals

Table 38: SAI2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.66		sai2.MCLK	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ29
J2.62		sai2.RX_BCLK	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ31
J2.73		sai2.RX_DATA[0]	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG29
J2.78		sai2.RX_DATA[1]	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); Internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise. This sets boot source.	AF28
J2.67		sai2.RX_DATA[2]	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG27
J2.70		sai2.RX_DATA[3]	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG25
J1.40		sai2.RX_DATA[4]	1	Runs @ 1.8V	AJ43
J1.34		sai2.RX_DATA[5]	1	Runs @ 1.8V	AJ41
J1.38		sai2.RX_DATA[6]	3	Runs @ 1.8V	AK44
J2.57		sai2.RX_DATA[6]	3	Runs @ 1.8V	AK50
J1.47		sai2.RX_DATA[7]	3	Runs @ 1.8V	AH42
J2.59		sai2.RX_DATA[7]	3	Runs @ 1.8V	AJ51
J2.63		sai2.RX_SYNC	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK32
J2.71		sai2.TX_BCLK	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG23
J2.64		sai2.TX_DATA[0]	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AH26
J2.72		sai2.TX_DATA[1]	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ25
J2.65		sai2.TX_DATA[2]	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ27
J2.69		sai2.TX_DATA[3]	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK28
J1.48		sai2.TX_DATA[4]	1	Runs @ 1.8V	AJ45
J1.32		sai2.TX_DATA[5]	1	Runs @ 1.8V	AH46
J1.50		sai2.TX_DATA[6]	1	Runs @ 1.8V	AJ47
J1.46		sai2.TX_DATA[7]	1	Runs @ 1.8V	AK48
J2.74		sai2.TX_SYNC	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AF24

8.8.2.4 SAI3 Signals

Table 39: SAI3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.16	no AC	sai3.MCLK	1		P48
J2.08	no AC	sai3.RX_BCLK	1		P52
J2.14	no AC	sai3.RX_BCLK	7		R51
J2.02	no AC	sai3.RX_DATA[0]	1		R49
J2.06	no AC	sai3.RX_SYNC	1		R45
J2.86		sai3.RX_SYNC	7		N45
J2.04	no AC	sai3.TX_BCLK	1		P46
J2.06	no AC	sai3.TX_DATA[0]	7		R45
J2.14	no AC	sai3.TX_DATA[0]	1		R51

8.8.2.5 SAI4 Signals

Table 40: SAI4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.34		sai4.RX_BCLK	2	Runs @ 1.8V	AJ41
J2.65		sai4.RX_BCLK	3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ27
J1.46		sai4.RX_DATA[0]	2	Runs @ 1.8V	AK48
J2.69		sai4.RX_DATA[0]	3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK28
J1.48		sai4.RX_DATA[1]	3	Runs @ 1.8V	AJ45
J1.40		sai4.RX_SYNC	2	Runs @ 1.8V	AJ43
J2.72		sai4.RX_SYNC	3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ25
J1.48		sai4.TX_BCLK	2	Runs @ 1.8V	AJ45
J2.67		sai4.TX_BCLK	3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG27
J1.50		sai4.TX_DATA[0]	2	Runs @ 1.8V	AJ47
J2.70		sai4.TX_DATA[0]	3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG25
J1.32		sai4.TX_DATA[1]	3	Runs @ 1.8V	AH46
J1.32		sai4.TX_SYNC	2	Runs @ 1.8V	AH46
J2.78		sai4.TX_SYNC	3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); Internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise. This sets boot source.	AF28

8.8.2.6 SAI5 Signals

Table 41: SAI5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.47		sai5.RX_BCLK	1	Runs @ 1.8V	AH42
J2.35	SDEX	sai5.RX_BCLK	3	Available in "SDEX" configuration; Runs @ 1.8V	AG49
J2.45	SDEX	sai5.RX_DATA[0]	3	Available in "SDEX" configuration; Runs @ 1.8V	AG51
J2.61		sai5.RX_DATA[0]	1	Runs @ 1.8V	AH50
J2.33	SDEX	sai5.RX_DATA[1]	2	Available in "SDEX" configuration; Runs @ 1.8V	AH52
J2.55		sai5.RX_DATA[1]	2	Runs @ 1.8V	AJ49
J2.31	SDEX	sai5.RX_DATA[2]	2	Available in "SDEX" configuration; Runs @ 1.8V	AE49
J2.57		sai5.RX_DATA[2]	2	Runs @ 1.8V	AK50
J2.29	SDEX	sai5.RX_DATA[3]	2	Available in "SDEX" configuration; Runs @ 1.8V	AF52
J2.59		sai5.RX_DATA[3]	2	Runs @ 1.8V	AJ51
J1.38		sai5.RX_SYNC	1	Runs @ 1.8V	AK44
J2.43	SDEX	sai5.RX_SYNC	3	Available in "SDEX" configuration; Runs @ 1.8V	AF48
J2.29	SDEX	sai5.TX_BCLK	3	Available in "SDEX" configuration; Runs @ 1.8V	AF52
J2.59		sai5.TX_BCLK	1	Runs @ 1.8V	AJ51
J2.33	SDEX	sai5.TX_DATA[0]	3	Available in "SDEX" configuration; Runs @ 1.8V	AH52
J2.55		sai5.TX_DATA[0]	1	Runs @ 1.8V	AJ49
J2.45	SDEX	sai5.TX_DATA[1]	2	Available in "SDEX" configuration; Runs @ 1.8V	AG51
J2.61		sai5.TX_DATA[1]	2	Runs @ 1.8V	AH50
J1.38		sai5.TX_DATA[2]	2	Runs @ 1.8V	AK44
J2.43	SDEX	sai5.TX_DATA[2]	2	Available in "SDEX" configuration; Runs @ 1.8V	AF48
J1.47		sai5.TX_DATA[3]	2	Runs @ 1.8V	AH42
J2.35	SDEX	sai5.TX_DATA[3]	2	Available in "SDEX" configuration; Runs @ 1.8V	AG49
J2.31	SDEX	sai5.TX_SYNC	3	Available in "SDEX" configuration; Runs @ 1.8V	AE49
J2.57		sai5.TX_SYNC	1	Runs @ 1.8V	AK50

8.8.3 PDM - Microphone Interface (MICFIL)

The PDM module of the iMX 95 SOC provides a popular way to deliver audio from microphones to the processor in several applications, such as mobile telephones. Up to 8 channels can be implemented with 4 lanes.

PDM includes the following Features:

- Decimation filters:
  - Fixed-point filtering
  - 24-bit PCM audio output
  - Internal clock divider for a programmable PDM clock generation:
  - Frame synchronization
  - Full or partial set of channel operations with individual enable controls
  - Programmable decimation rate
  - Programmable DC remover
  - Programmable DC remover at output
  - Range adjustment capability
- FIFOs with interrupt and DMA capability: each FIFO having a length of 32 entries
- Hardware voice activity detector (HWVAD), equipped with:
  - Interrupt capability
  - Zero-crossing detection (ZCD) option

MICFILE is in AON domain.

8.8.3.1 PDM Signals

Table 42: PDM Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.02	no AC	pdm.BIT_STREAM[0]	2		R49
J2.56		pdm.BIT_STREAM[0]	0		G45
J2.81		pdm.BIT_STREAM[0]	2		L45
J2.10	no AC	pdm.BIT_STREAM[1]	2		U45
J2.48		pdm.BIT_STREAM[1]	0		H46
J2.83		pdm.BIT_STREAM[1]	2		L49
J2.04	no AC	pdm.BIT_STREAM[2]	2		P46
J2.86		pdm.BIT_STREAM[2]	2		N45
J2.06	no AC	pdm.BIT_STREAM[3]	2		R45
J2.85		pdm.BIT_STREAM[3]	2		N49
J2.14	no AC	pdm.CLK	2		R51
J2.50		pdm.CLK	0		F46
J2.79		pdm.CLK	2		K46

8.8.4 SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

SPDIF is in Wakeup domain.

8.8.4.1 SPDIF Signals

Table 43: SPDIF Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.60		spdif1.IN	2	Duplicate pin on J3.28	T44
J2.68		spdif1.IN	2	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AH30
J2.69		spdif1.IN	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK28
J3.28		spdif1.IN	2	Duplicate pin on J2.60	T44
J2.54		spdif1.OUT	2	Duplicate pin on J3.36	T46
J2.68		spdif1.OUT	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AH30
J3.36		spdif1.OUT	2	Duplicate pin on J2.54	T46

8.8.5 MQS – Medium Quality Sound

Medium quality sound (MQS) is used to generate medium quality audio via a standard GPIO in the pinmux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip.

MQS1 is in AON domain, MQS2 is in NETC domain.

8.8.5.1 MQS1 Signals

Table 44: MQS1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.13		mqs1.LEFT	4	Duplicate pin on J2.42 BOOT_MODE2 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull down; GPIO can be output only or tristated.	G49
J2.42		mqs1.LEFT	4	Duplicate pin on J2.13; see J2.13 note	G49
J2.50		mqs1.LEFT	1		F46
J2.36		mqs1.RIGHT	4		H52
J2.56		mqs1.RIGHT	1		G45

8.8.5.2 MQS2 Signals

Table 45: MQS2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.84		mqs2.LEFT	2	Will change level according to J1.90 VDD_SDIO2;	AA49
J2.07		mqs2.LEFT	1	Runs @ 1.8V	AK24
J2.68		mqs2.LEFT	3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AH30
J1.78		mqs2.RIGHT	2	Will change level according to J1.90 VDD_SDIO2;	AA51
J2.09		mqs2.RIGHT	1	Runs @ 1.8V	AJ23
J2.66		mqs2.RIGHT	3	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ29

8.8.6 Audio transceiver signals

The following Audio transceiver differential pair is exported from SOM

Table 46: AUD Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.27		AUD_N_HPD	0	Differential Pair Negative side	Y46
J2.25		AUD_P_UTIL	0	Differential Pair Positive side	Y44

8.9 LPUART - Low Power Universal Asynchronous Receiver/Transmitter

The DART-MX95 exposes up to 8 LPUART interfaces available by the i.MX95 SOC. LPUART5 is used on SOM for Bluetooth interface and can be accessible only if the on SOM buffer disabled or without ***"WBD", "WBE" Configurations***.

LPUART includes the following features:

- Full-duplex, standard NRZ format
- Programmable baud rates (13-bit modulo divider) with a configurable oversampling ratio (OSR) from 4× to 32×
- Asynchronous operation of transmit and receive baud rates with respect to the bus clock:
    - Baud rate can be configured independently of the bus clock frequency.
    - Operation in Low-Power modes is supported.
- Interrupt, DMA, or polled operations:
    - Transmit data empty and transmission complete
    - Receive data full
    - Receive overrun, parity error, framing error, and noise error
    - Idle receiver detect
    - Active edge on receive pin
    - Break detect supporting LIN
    - Receive data match
- Hardware parity generation and checking
- Programmable 7-bit, 8-bit, 9-bit, or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Support for three receiver wake-up methods:
    - Idle line wake-up
    - Address mark wake-up
    - Receive data match
- Automatic address matching to reduce ISR overhead:
    - Address mark matching
    - Idle line address matching
    - Address match start, address match end
- Optional 13-bit and 11-bit break character generation
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64, or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with a programmable pulse width
- Independent FIFO structure for transmit and receive functions:
    - Separate configurable watermarks for receive and transmit requests

- Option for receiver to assert request after a configurable number of idle characters, if receive FIFO is not empty

LPUART1-LPUART2 are in AON domain, LPUART3-LPUART8 are in Wakeup domain.

Table 47: LPUART I/O Signals

NAME	FUNCTION	DIR
TXD	Transmit data: This pin is normally an output, but is an input (tristated) in Single-Wire mode whenever the transmitter is disabled or the transmit direction is configured for receive data	I/O
RXD	Receive data	I
CTS_B	Clear-to-send	I
RTS_B	Request-to-send	O
DTR_B	Data terminal ready	O
DSR_B	Data set ready	I
DCD_B	Data carrier detect	I
RIN_B	Ring indicator	I

8.9.1 LPUART1 Signals

Table 48: LPUART1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.46		uart1.CTS_B	1		E51
J2.38		uart1.DSR_B	3		G51
J1.72		uart1.DTR_B	3	Duplicate pin on J2.44 BOOT_MODE3 pin, Has internal 10K PU to J1.27 (3.3V); Do not drive until after POR_B rise + 30ms; GPIO can be output only or tristated.	H48
J2.44		uart1.DTR_B	3	Duplicate pin on J1.72; see J1.72 note	H48
J2.11		uart1.RTS_B	1	Duplicate pin on J3.50 (In initial SOM Rev 1.0 on pin J3.48); BOOT_MODE1 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull up to J1.27 (3.3V); GPIO can be output only or tristated.	F48
J3.50		uart1.RTS_B	1	Duplicate pin on J2.11; see J2.11 note (In initial SOM Rev 1.0 exported on pin J3.48)	F48
J2.88		uart1.RX	0	Used as console debug on Variscite release;	E49
J2.90		uart1.TX	0	Used as console debug on Variscite release; BOOT_MODE0 pin, Do not drive until after POR_B rise + 30ms; Internal buffer connected to J2.78 drives this pin, latched with POR_B rise; This sets boot source. GPIO can be output only or tristated.	F52

8.9.2 LPUART2 Signals

Table 49: LPUART2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.38		uart2.CTS_B	1		G51
J2.34		uart2.DCD_B	2		E43
J2.36		uart2.DSR_B	3		H52

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.13		uart2.DTR_B	3	Duplicate pin on J2.42 BOOT_MODE2 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull down; GPIO can be output only or tristated.	G49
J2.42		uart2.DTR_B	3	Duplicate pin on J2.13; see J2.13 note	G49
J2.40		uart2.RIN_B	2		E45
J1.72		uart2.RTS_B	1	Duplicate pin on J2.44 BOOT_MODE3 pin, Has internal 10K PU to J1.27 (3.3V); Do not drive until after POR_B rise + 30ms; GPIO can be output only or tristated.	H48
J2.44		uart2.RTS_B	1	Duplicate pin on J1.72; see J1.72 note	H48
J2.46		uart2.RX	0		E51
J2.11		uart2.TX	0	Duplicate pin on J3.50 (In initial SOM Rev 1.0 on pin J3.48); BOOT_MODE1 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull up to J1.27 (3.3V); GPIO can be output only or tristated.	F48
J3.50		uart2.TX	0	Duplicate pin on J2.11; see J2.11 note (In initial SOM Rev 1.0 exported on pin J3.48)	F48

8.9.3 LPUART3 Signals

Table 50: LPUART3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.12	no EC	uart3.CTS_B	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AK36
J2.04	no AC	uart3.CTS_B	4		P46
J1.13		uart3.DCD_B	1	Runs @ 3.3V level via NTS0104GU12 level translator	AK40
J1.09	no EC	uart3.DSR_B	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AH34
J1.03	no EC	uart3.DTR_B	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AF32
J1.11		uart3.RIN_B	1	Runs @ 3.3V level via NTS0104GU12 level translator	AJ39
J1.02	no EC	uart3.RTS_B	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG35
J2.16	no AC	uart3.RTS_B	4		P48
J1.10	no EC	uart3.RX	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AJ35
J2.87		uart3.RX	1		P44
J1.04	no EC	uart3.TX	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG33
J2.89		uart3.TX	1		N51

8.9.4 LPUART4 Signals

Table 51: LPUART4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.04	no AC	uart4.CTS_B	6		P46
J2.66		uart4.CTS_B	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ29

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.63		uart4.DCD_B	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK32
J2.64		uart4.DSR_B	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AH26
J2.74		uart4.DTR_B	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AF24
J2.62		uart4.RIN_B	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ31
J2.16	no AC	uart4.RTS_B	6		P48
J2.67		uart4.RTS_B	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG27
J2.65		uart4.RX	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ27
J2.87		uart4.RX	6		P44
J2.70		uart4.TX	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG25
J2.89		uart4.TX	6		N51

8.9.5 LPUART5 Signals

Table 52: LPUART5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.01		uart5.CTS_B	6	Add external 10K pull down; Runs @ 1.8V	AG21
J2.26		uart5.CTS_B	5	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K48
J2.03		uart5.RTS_B	6	Runs @ 1.8V	AH22
J2.22		uart5.RTS_B	5	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K52
J2.07		uart5.RX	6	Runs @ 1.8V	AK24
J2.24		uart5.RX	5	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J51
J2.09		uart5.TX	6	Runs @ 1.8V	AJ23
J2.20		uart5.TX	5	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J49

8.9.6 LPUART6 Signals

Table 53: LPUART6 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.83		uart6.CTS_B	5		L49
J3.52		uart6.CTS_B	2		W49
J2.77		uart6.RTS_B	5		L51
J3.58		uart6.RTS_B	2		W51
J2.81		uart6.RX	5		L45
J3.48		uart6.RX	2	(In initial SOM Rev 1.0 exported on pin J3.50)	W45
J2.79		uart6.TX	5		K46
J3.38		uart6.TX	2		V52

8.9.7 LPUART7 Signals

Table 54: LPUART7 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.19		uart7.CTS_B	5		M48
J1.17		uart7.RTS_B	5		M52
J3.03		uart7.RX	5		M46
J3.62		uart7.RX	2		Y52
J3.01		uart7.TX	5		M44

8.9.8 LPUART8 Signals

Table 55: LPUART8 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.89		uart8.CTS_B	5		N51
J2.87		uart8.RTS_B	5		P44
J2.85		uart8.RX	5		N49
J2.86		uart8.TX	5		N45

8.10 LPSPI - Low Power Serial Peripheral Interface

The DART-MX95 exposes up to 8 LPSPI interfaces available by the i.MX95 SOC.
LPSPI provides an efficient interface (either as a master or slave) to an SPI bus, which is a synchronous serial communication interface used in embedded systems. It is typically used to perform short distance communications between microcontrollers and peripheral devices, on printed circuit boards. Typical applications include interfacing with secure digital cards and LCD displays.

LPSPI includes the following Features:

- Minimal CPU overhead, with DMA transmit and receive requests supporting FIFO register accesses
- Support available for 32-bit word size
- Configurable clock polarity and phase
- Support available for 2 peripheral chip selects in Master mode
- Support available for Slave mode
- 16-word transmit and command FIFO
- 16-word receive FIFO
- Flexible timing parameters in Master mode, including SCK frequency and duty cycle, and delays between PCS and SCK edges
- Continuous transfer option to keep PCS asserted across multiple frames
- Full-duplex transfers that support 1-bit transmit and receive on each clock edge
- Half-duplex transfers that support:
    - 1-bit transmit or receive on each clock edge

There are two instances of the LPSPI in the Always-on (AON) domain: LPSPI1, LPSPI2.
Each of these LPSPI instances supports the SPI Master mode only.
In Wakeup domain, there are six LPSPI instances: LPSPI3- LPSPI8
The LPSPI instances of Wakeup domain support both Master mode and Slave mode.

8.10.1 LPSPI1 Signals

Table 56: LPSPI1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.13		spi1.PCS0	2	Duplicate pin on J2.42 BOOT_MODE2 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull down; GPIO can be output only or tristated.	G49
J2.42		spi1.PCS0	2	Duplicate pin on J2.13; see J2.13 note	G49
J2.56		spi1.PCS1	2		G45
J1.72		spi1.SCK	2	Duplicate pin on J2.44 BOOT_MODE3 pin, Has internal 10K PU to J1.27 (3.3V); Do not drive until after POR_B rise + 30ms; GPIO can be output only or tristated.	H48
J2.44		spi1.SCK	2	Duplicate pin on J1.72; see J1.72 note	H48
J2.38		spi1.SIN	2		G51
J2.36		spi1.SOUT	2		H52

8.10.2 LPSPI2 Signals

Table 57: LPSPI2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.90		spi2.PCS0	2	Used as console debug on Variscite release; BOOT_MODE0 pin, Do not drive until after POR_B rise + 30ms; Internal buffer connected to J2.78 drives this pin, latched with POR_B rise; This sets boot source. GPIO can be output only or tristated.	F52
J2.48		spi2.PCS1	2		H46
J2.11		spi2.SCK	2	Duplicate pin on J3.50 (In initial SOM Rev 1.0 on pin J3.48); BOOT_MODE1 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull up to J1.27 (3.3V); GPIO can be output only or tristated.	F48
J3.50		spi2.SCK	2	Duplicate pin on J2.11; see J2.11 note (In initial SOM Rev 1.0 exported on pin J3.48)	F48
J2.88		spi2.SIN	2	Used as console debug on Variscite release;	E49
J2.46		spi2.SOUT	2		E51

8.10.3 LPSPI3 Signals

Table 58: LPSPI3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.01		spi3.PCS0	1		M44
J2.77		spi3.PCS1	1		L51
J1.17		spi3.SCK	1		M52
J3.03		spi3.SIN	1		M46
J1.19		spi3.SOUT	1		M48

8.10.4 LPSPI4 Signals

Table 59: LPSPI4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.08	no AC	spi4.PCS0	5		P52
J3.52		spi4.PCS0	4		W49
J2.16	no AC	spi4.PCS1	5		P48
J3.48		spi4.PCS1	4	(In initial SOM Rev 1.0 exported on pin J3.50)	W45
J2.04	no AC	spi4.PCS2	5		P46
J3.38		spi4.PCS2	4		V52
J2.14	no AC	spi4.SCK	5		R51
J3.62		spi4.SCK	4		Y52
J2.06	no AC	spi4.SIN	5		R45
J3.58		spi4.SIN	4		W51
J2.02	no AC	spi4.SOUT	5		R49

8.10.5 LPSPI5 Signals

Table 60: LPSPI5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.08	no AC	spi5.PCS0	4		P52
J2.14	no AC	spi5.SCK	4		R51
J2.06	no AC	spi5.SIN	4		R45
J2.02	no AC	spi5.SOUT	4		R49

8.10.6 LPSPI6 Signals

Table 61: LPSPI6 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.20		spi6.PCS0	4	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J49
J3.54		spi6.PCS1	6		T48
J2.22		spi6.SCK	4	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K52
J2.24		spi6.SIN	4	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J51
J2.26		spi6.SOUT	4	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K48

8.10.7 LPSPI7 Signals

Table 62: LPSPI7 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.79		spi7.PCS0	4		K46
J3.64		spi7.PCS1	6		T52
J2.77		spi7.SCK	4		L51
J2.81		spi7.SIN	4		L45
J2.83		spi7.SOUT	4		L49

8.10.8 LPSPI8 Signals

Table 63: LPSPI8 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.86		spi8.PCS0	4		N45
J2.10	no AC	spi8.PCS1	6		U45
J2.87		spi8.SCK	4		P44
J2.85		spi8.SIN	4		N49
J2.89		spi8.SOUT	4		N51

8.11 FlexSPI - Flexible Serial Peripheral Interface

DART-MX95 exposes The FlexSPI module which can interface to one external Octal serial flash device, or up to two external Quad SPI serial flash devices, each up to four bidirectional data lines. Both Serial NOR flash and Serial NAND flash are supported.

The FlexSPI module acts as an interface to external serial flash devices.
Note: Only signals exported on **ALT0** can be used for boot through FlexSPI.

FlexSPI includes the following Features:

- Flexible sequence engine (lookup table) to support various vendor devices
  - Serial NOR flash memory and other devices with SPI protocol similar to serial NOR flash memory
  - Serial NAND flash memory
  - HyperBus devices (HyperFlash/HyperRAM)
  - XCCELA devices
  - FPGA devices
- Flash memory access modes
  - Single, Dual, Quad, Octal mode
  - Single Data Transfer Rate (SDR) and Double Data Transfer Rate (DDR) mode
  - Individual mode
- Sampling clock mode
  - Internal dummy read strobe looped back internally
  - Internal dummy read strobe looped back from pad
  - SCLK clock output looped back from pad
  - Flash-memory-provided read strobe
- Automatic data learning to select the correct sample clock phase
- Memory mapped read and write access by AHB bus
  - AHB receive buffer implemented to reduce read latency. See the chip-specific section for AHB buffer size.
  - 16 AHB controllers with programmable priority for read access from each
  - 8 flexible and configurable buffers in AHB receive buffer
  - AHB transmit buffer implemented to buffer all write data from one AHB burst. See the chip-specific section for AHB buffer size.
    Note: All AHB controllers share this AHB transmit buffer. There is no AHB controller number limitation for write access.
- Software-triggered flash memory read and write access by IP bus
  - IP receive FIFO implemented to buffer all read data from external devices. FIFO size: 512 bytes
  - IP transmit FIFO implemented to buffer all write data to external devices. FIFO size: 1024 bytes
  - DMA support to read IP receive FIFO
  - DMA support to fill IP transmit FIFO
  - SCLK stops when IP receive FIFO is full during reading flash memory data
  - SCLK stops when IP transmit FIFO is empty during writing flash memory data

8.11.1 FlexSPI Signals

Table 64: FlexSPI Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.48		flexspi.A_DATA[0]	0	Runs @ 1.8V	AJ45
J2.35	SDEX	flexspi.A_DATA[0]	1	Available in "SDEX" configuration; Runs @ 1.8V	AG49
J1.32		flexspi.A_DATA[1]	0	Runs @ 1.8V	AH46
J2.33	SDEX	flexspi.A_DATA[1]	1	Available in "SDEX" configuration; Runs @ 1.8V	AH52
J1.50		flexspi.A_DATA[2]	0	Runs @ 1.8V	AJ47
J2.31	SDEX	flexspi.A_DATA[2]	1	Available in "SDEX" configuration; Runs @ 1.8V	AE49
J1.46		flexspi.A_DATA[3]	0	Runs @ 1.8V	AK48
J2.29	SDEX	flexspi.A_DATA[3]	1	Available in "SDEX" configuration; Runs @ 1.8V	AF52
J2.55		flexspi.A_DATA[4]	0	Runs @ 1.8V	AJ49
J2.57		flexspi.A_DATA[5]	0	Runs @ 1.8V	AK50
J2.59		flexspi.A_DATA[6]	0	Runs @ 1.8V	AJ51
J2.61		flexspi.A_DATA[7]	0	Runs @ 1.8V	AH50
J1.38		flexspi.A_DQS	0	Runs @ 1.8V	AK44
J1.40		flexspi.A_SCLK	0	Runs @ 1.8V	AJ43
J2.45	SDEX	flexspi.A_SCLK	1	Available in "SDEX" configuration; Runs @ 1.8V	AG51
J1.34		flexspi.A_SS0_B	0	Runs @ 1.8V	AJ41
J2.43	SDEX	flexspi.A_SS0_B	1	Available in "SDEX" configuration; Runs @ 1.8V	AF48
J1.47		flexspi.A_SS1_B	0	Runs @ 1.8V	AH42
J1.40		xspi_slv.CLK	4	Runs @ 1.8V	AJ43
J2.45	SDEX	xspi_slv.CLK	6	Available in "SDEX" configuration; Runs @ 1.8V	AG51
J1.34		xspi_slv.CS	4	Runs @ 1.8V	AJ41
J2.43	SDEX	xspi_slv.CS	6	Available in "SDEX" configuration; Runs @ 1.8V	AF48
J1.48		xspi_slv.DATA[0]	4	Runs @ 1.8V	AJ45
J2.35	SDEX	xspi_slv.DATA[0]	6	Available in "SDEX" configuration; Runs @ 1.8V	AG49
J1.32		xspi_slv.DATA[1]	4	Runs @ 1.8V	AH46
J2.33	SDEX	xspi_slv.DATA[1]	6	Available in "SDEX" configuration; Runs @ 1.8V	AH52
J1.50		xspi_slv.DATA[2]	4	Runs @ 1.8V	AJ47
J2.31	SDEX	xspi_slv.DATA[2]	6	Available in "SDEX" configuration; Runs @ 1.8V	AE49
J1.46		xspi_slv.DATA[3]	4	Runs @ 1.8V	AK48
J2.29	SDEX	xspi_slv.DATA[3]	6	Available in "SDEX" configuration; Runs @ 1.8V	AF52
J2.55		xspi_slv.DATA[4]	4	Runs @ 1.8V	AJ49
J2.57		xspi_slv.DATA[5]	4	Runs @ 1.8V	AK50
J2.59		xspi_slv.DATA[6]	4	Runs @ 1.8V	AJ51
J2.61		xspi_slv.DATA[7]	4	Runs @ 1.8V	AH50
J1.38		xspi_slv.DQS	4	Runs @ 1.8V	AK44

8.12 LPI2C - Low Power Inter-Integrated Circuit

The DART-MX95 SOM exposes up to seven LPI2C interfaces available by the i.MX95 SOC.

LPI2C supports an efficient interface to an I2C bus as a controller and target:

- Implements logic support for Standard, Fast, Fast+, HS-mode (target only) and Ultra-Fast modes of operation
- Uses little CPU overhead, with DMA offloading of FIFO register accesses

LPI2C also complies with the System Management Bus (SMBus) Specification, version 3. The SMBus is a single-ended simple two-wire bus, which is typically used for low-bandwidth communications.

The Inter-Integrated Circuit (I2C) serial bus is multi-controller, multi-target, packet-switched, and single-ended, and is often used to attach microcontroller ICs to lower-speed peripheral ICs.

LPI2C supports:

- Standard, Fast, Fast+ and Ultra Fast modes
- HS mode in target mode
- Multicontroller, including synchronization and arbitration, means that any number of controller nodes can be present. Also, controller and target roles can be changed between messages (after a Stop signal is sent).
- Clock stretching. Used on the SCL line, as an I2C flow control mechanism.
- Arbitration for when the system has more than one controller. When used on the SDA line, ensures that there is only one I2C transmitter at a time.
- General call, seven-bit addressing, and ten-bit addressing
- Software reset, Start byte, and device ID (also require software support)

The LPI2C controller supports:

- Command and transmit FIFO of 8 words (8-bit transmit data + 3-bit command)
- Receive FIFO of 8 words (8-bit receive data).
- Command FIFO waiting for an I2C idle bus before initiating a transfer
- Initiation of repeated Start and Stop conditions and one or more controller-receiver transfers by command FIFO
- Stop condition generation from command FIFO, or automatic generation of Stop condition when the transmit FIFO is empty
- Interrupt generation on data match and unwanted data rejection, via flexible receive data match
- Flags and optional interrupt signals at repeated Start condition, Stop condition, loss of arbitration, unexpected NACK, and command word errors
- Configurable bus idle timeout and pin-stuck-low timeout

The LPI2C target supports:

- Separate I2C target registers to minimize software overhead because of controller or target switching
- 7-bit or 10-bit addressing, address range, SMBus alert, and general call address.

- Transmit data register that supports interrupt or DMA requests
- Receive data register that supports interrupt or DMA requests
- Software-controllable ACK or NACK, with optional clock stretching on ACK or NACK field
- Configurable clock stretching, to avoid transmit-FIFO-underrun and receive-FIFO-overrun errors
- Flags and optional interrupt at end of packet, Stop condition, or bit error detection

The AON domain supports two LPI2C (LPI2C1, LPI2C2) slave instances - LPI2C1 is internal to SOM while LPI2C1 is exported.
The Wakeup domain supports six LPI2C (LPI2C3- LPI2C8).
The LPI2C instances of Wakeup domain support both Master mode and Slave mode.

8.12.1 LPI2C2 Signals

Table 65: LPI2C2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.34		i2c2.SCL	0		E43
J2.40		i2c2.SDA	0		E45

8.12.2 LPI2C3 Signals

Table 66: LPI2C3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.24		i2c3.SCL	1	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J51
J2.32		i2c3.SCL	1		V44
J2.20		i2c3.SDA	1	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J49
J2.30		i2c3.SDA	1		U51

8.12.3 LPI2C4 Signals

Table 67: LPI2C4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.22		i2c4.SCL	1	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K52
J3.46		i2c4.SCL	1	Pin has 4.99K pull up on DART	V48
J2.26		i2c4.SDA	1	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K48
J3.42		i2c4.SDA	1	Pin has 4.99K pull up on DART	V46

8.12.4 LPI2C5 Signals

Table 68: LPI2C5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.24		i2c5.SCL	6	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J51
J2.54		i2c5.SCL	6	Duplicate pin on J3.36	T46
J3.36		i2c5.SCL	6	Duplicate pin on J2.54	T46
J2.20		i2c5.SDA	6	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J49
J2.60		i2c5.SDA	6	Duplicate pin on J3.28	T44
J3.28		i2c5.SDA	6	Duplicate pin on J2.60	T44

8.12.5 LPI2C6 Signals

Table 69: LPI2C6 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.22		i2c6.SCL	6	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K52
J2.81		i2c6.SCL	6		L45
J2.26		i2c6.SDA	6	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K48
J2.79		i2c6.SDA	6		K46

8.12.6 LPI2C7 Signals

Table 70: LPI2C7 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.77		i2c7.SCL	6		L51
J3.03		i2c7.SCL	6		M46
J2.83		i2c7.SDA	6		L49
J3.01		i2c7.SDA	6		M44

8.12.7 LPI2C8 Signals

Table 71:LPI2C8 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.17		i2c8.SCL	6		M52
J2.85		i2c8.SCL	6		N49
J1.19		i2c8.SDA	6		M48

8.13 I3C

The DART-MX95 exports one I3C serial interface. I3C is a communications processor that improves upon the use and power of I2C, and provides an alternative to SPI for mid-speed applications.

I3C main features are:

- Two-wire multidrop bus that is capable of 12.5 MHz clock speeds with up to 11 devices:
  - Uses standard pads with 4 mA drive.
  - Dynamically assigns target addresses, and targets do not require static addresses (SAs). However, targets can have an I2C static address assigned at startup, so the target can operate on an I2C bus. By default, I3C supports 7-bit I2C-style addresses.
  - Supports extended I2C 10-bit addressing through Map Feature Control 1 (SMAPCTRL1).
  - Allows targets to use the inbound SCL clock as the peripheral clock (instead of the clock from the controller) so that devices can have slow or inaccurate clocks internally.
  - Allows simple targets, such as temperature sensors, to have no internal clock.
  - I3C controller supports handoff from Open-Drain to Push-Pull mode for ACK to data transfer.
  - Generally, the controller terminates the read, but for I3C, the target can also end the read.
- IBIs that allow targets to send notifications to a controller:
  - Can be equivalent to a separate GPIO, but can also be directly data-bearing.
  - Can be prioritized. When multiple targets send interrupts to a controller at the same time, the order is resolved. Dynamic addresses (DAs) establish the priority of the targets, so the controller controls the priority of the targets. Targets with lower-value DAs are higher-priority level IBIs.
  - Can start interrupts even when the controller is not active on the bus. A free-running clock is not required, but starting an interrupt requires a Bus Available condition.\
  - Can resolve an initial event via a time-stamping option, not requiring an interrupt.
- Built-in commands for applications created in software or firmware by using the register interface maintained in a separate space. These commands do not collide with normal controller-to-target messages and:
  - Control bus behavior, modes and states, low-power state, inquiries, and more.
  - Have an extra room for new built-in commands for other groups.
- Organized forms of multicontroller modes that are secondary controllers using clean handoffs between different controllers.

- Hot-Join onto I3C bus allows devices to connect to the bus later than when the bus starts. This:
  - Enables a device or module to access the I3C bus after power up or when physically inserted onto the I3C bus.
  - Provides a clean method for notification when new devices or modules access the I3C bus.
- I3C can use both I2C and I3C buses:
  - I3C supports specific legacy I2C devices on the bus.
  - I3C target devices can operate on I2C buses.
  - I3C supports bridging to I2C, SPI, UART, and other buses.
- Higher data rate modes are available:
  - I3C has a high data rate: double data rate (HDR-DDR) mode, which is double the data rate of SDR.
  - Only the controller and the specific target must support the higher data rate (the other targets can ignore it).

I3C2 is in AON domain.

8.13.1 I3C Signals

Table 72: I3C Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.02	no EC	i3c2.PUR	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG35
J1.88		i3c2.PUR	2	Will change level according to J1.90 VDD_SDIO2;	AB52
J1.02	no EC	i3c2.PUR_B	6	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG35
J1.88		i3c2.PUR_B	3	Will change level according to J1.90 VDD_SDIO2;	AB52
J1.13		i3c2.SCL	2	Runs @ 3.3V level via NTS0104GU12 level translator	AK40
J1.74		i3c2.SCL	2	External SD card detect input; Add 10K external pull up to J1.90; Will change level according to J1.90 VDD_SDIO2;	AD48
J1.11		i3c2.SDA	2	Runs @ 3.3V level via NTS0104GU12 level translator	AJ39
J1.82		i3c2.SDA	2	Will change level according to J1.90 VDD_SDIO2;	AB48

8.14 FlexCAN - Flexible Data Rate CAN

The DART-MX95 exports up to five FlexCAN modules available by the i.MX95 SOC.

FlexCAN is a communication controller implementing the CAN protocol according to the ISO 11898-1:2015 standard and CAN 2.0 Part B protocol specifications.

The CAN protocol was primarily designed to be used as a vehicle serial data bus, meeting the specific real-time processing and reliable operation requirements in the electromagnetic interference (EMI) environment of a vehicle. FlexCAN is a full implementation of the CAN protocol specification, the CAN with flexible data rate (CAN FD) protocol, and the CAN version 2.0 Part B protocol. It supports both standard and extended message frames and long payloads.

FlexCAN includes the following features:

- Full implementation of CAN with Flexible data rate (CAN FD) protocol specification and CAN Specification Version 2.0, Part B
    - Standard data frames
    - Extended data frames
    - Data length of 0–64 bytes
    - Content-related addressing
- Compliance with ISO 11898-1:2015 standard
- Flexible message buffers that can be configured to store a payload of 0, 8, 16, 32, or 64 bytes
    - Increasing the payload size decreases the number of supported message buffers (see FlexCAN memory partition for CAN FD).
    - Message buffers are configurable as receive or transmit, supporting standard and extended messages.
- Individual Receive Mask registers for each message buffer
- Full-featured Legacy RX FIFO with storage capacity for six frames and automatic internal pointer handling with DMA support
- Full-featured Enhanced RX FIFO with storage capacity of 20 CAN FD frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Programmable clock source to CAN Protocol Interface, either peripheral clock or oscillator clock
- Optional general purpose RAM space, using RAM not used by reception or transmission structures
- Listen-Only mode
- Programmable loopback mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Timestamp based on 32-bit free-running timer, with optional external time tick
- Global network time, synchronized by specific message
- Maskable interrupts

- Independence from transmission medium (external transceiver is assumed)
- Short latency time due to arbitration scheme for high-priority messages
- Low-power modes, with programmable wake-up on bus activity
- Transceiver delay compensation when transmitting CAN FD messages at faster data rates
- Management of remote request frames, automatically or by software
- Restriction only to write CAN bit time settings and configuration bits in Freeze mode
- Transmit message buffer status (lowest-priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- ESR1[SYNCH] to indicate module is synchronous with CAN bus
- CRC status for transmitted message
- Legacy RX FIFO Global Mask register
- Selectable priority between message buffers and receive FIFO during matching process
- Powerful Legacy RX FIFO ID filtering, capable of matching incoming IDs against either 128 extended IDs, 256 standard IDs, or 512 partial (8-bit) IDs, with 32 individual masking capability
- Powerful Enhanced RX FIFO ID filtering, capable of matching incoming IDs against either 64 extended or 128 standard ID filter elements with three filtering schemes: mask plus filter, range, and two filters without mask.
- Complete backward compatibility with previous FlexCAN version
- Detection and correction of errors in memory read accesses.
    - Each byte of FlexCAN memory is associated to five parity bits.
    - The error correction mechanism ensures that errors in one bit of this 13-bit word can be corrected (correctable errors).
    - Errors in two bits can be detected but not corrected (noncorrectable errors).

FlexCAN1 is in AON domain, FlexCAN2-FlexCAN5 are in Wakeup domain.

8.14.1 FlexCAN1 Signals

Table 73:FlexCAN1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.38		can1.RX	4		G51
J2.56		can1.RX	6		G45
J1.72		can1.TX	4	Duplicate pin on J2.44 BOOT_MODE3 pin, Has internal 10K PU to J1.27 (3.3V); Do not drive until after POR_B rise + 30ms; GPIO can be output only or tristated.	H48
J2.44		can1.TX	4	Duplicate pin on J1.72; see J1.72 note	H48
J2.50		can1.TX	6		F46

8.14.2 FlexCAN2 Signals

Table 74: FlexCAN2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.06	no EC	can2.RX	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AF36
J1.80		can2.RX	2	Will change level according to J1.90 VDD_SDIO2;	AC49
J2.09		can2.RX	3	Runs @ 1.8V	AJ23
J1.08	no EC	can2.TX	2	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG37
J1.86		can2.TX	2	Will change level according to J1.90 VDD_SDIO2;	AC51
J2.07		can2.TX	3	Runs @ 1.8V	AK24
J3.64		can2.TX	2		T52

8.14.3 FlexCAN3 Signals

Table 75: FlexCAN3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.32		can3.RX	2		V44
J2.30		can3.TX	2		U51

8.14.4 FlexCAN4 Signals

Table 76: FlexCAN4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.01		can4.RX	2	Add external 10K pull down; Runs @ 1.8V	AG21
J2.81		can4.RX	3		L45
J2.03		can4.TX	2	Runs @ 1.8V	AH22
J2.79		can4.TX	3		K46

8.14.5 FlexCAN5 Signals

Table 77: FlexCAN5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.54		can5.RX	3	Duplicate pin on J3.36	T46
J3.36		can5.RX	3	Duplicate pin on J2.54	T46
J3.46		can5.RX	2	Pin has 4.99K pull up on DART	V48
J2.60		can5.TX	3	Duplicate pin on J3.28	T44
J3.28		can5.TX	3	Duplicate pin on J2.60	T44
J3.42		can5.TX	2	Pin has 4.99K pull up on DART	V46

8.15 Timer/PWM Module (TPM)

The DART-MX95 exports the 6 Timer/PWM modules available by the i.MX95 SOC.
TPM is a 4-channel timer that controls electric motor and power management applications by supporting:

- Input capture
- Output comparison
- Generation of PWM signals

An asynchronous clock that can remain enabled in low-power modes clocks the counter, compare, and capture registers.

Timer/PWM includes the following features:

- Supports selectable clock modes:
  - Can increment on every edge of the asynchronous counter clock
  - Can increment on the rising edge of an external clock input that is synchronized to the asynchronous counter clock
- Includes a prescaler divided by 1, 2, 4, 8, 16, 32, 64, or 128
- Includes a 32-bit TPM counter:
  - Can be a free-running counter or a modulo counter
  - The counting can be up or up-down
- Includes 4 channels that can be configured as follows:
  - Input Capture mode: the capture can occur on rising edges, falling edges, or both edges.
  - Output Compare mode: the output signal can be set, cleared, pulsed, or toggled on the match.
  - Edge-Aligned or Center-Aligned PWM mode for all channels.
- Supports the generation of an interrupt and DMA request per channel
- Supports the generation of an interrupt and DMA request when the counter overflows
- Supports selectable trigger input to either reset the counter to 0 or else cause the counter to start incrementing
  - The counter can also optionally stop incrementing on counter overflow.
- Supports the generation of hardware triggers when the counter overflows and per channel

TPM1-TPM2 are in AON domain, TPM3-TPM6 are in Wakeup domain.

8.15.1 TPM1 Signals

Table 78: TPM1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.88		tpm1.CH0	3	Used as console debug on Variscite release;	E49
J2.90		tpm1.CH1	3	Used as console debug on Variscite release; BOOT_MODE0 pin, Do not drive until after POR_B rise + 30ms; Internal buffer connected to J2.78 drives this pin,	F52

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				latched with POR_B rise; This sets boot source. GPIO can be output only or tristated.	
J2.46		tpm1.CH2	3		E51
J2.11		tpm1.CH3	3	Duplicate pin on J3.50 (In initial SOM Rev 1.0 on pin J3.48); BOOT_MODE1 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull up to J1.27 (3.3V); GPIO can be output only or tristated.	F48
J3.50		tpm1.CH3	3	Duplicate pin on J2.11; see J2.11 note (In initial SOM Rev 1.0 exported on pin J3.48)	F48
J2.56		tpm1.EXTCLK	3		G45

NOTE

Each TPM has its own clock root. TPM1_CH1 and TPM1_CH3 are only supported as outputs, not inputs. Features relying on channel inputs, such as input trigger, input capture or software compare are not supported on those channels.

8.15.2 TPM2 Signals

Table 79: TPM2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.34		tpm2.CH2	3		E43
J2.40		tpm2.CH3	3		E45
J2.48		tpm2.EXTCLK	3		H46

8.15.3 TPM3 Signals

Table 80: TPM3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.79		tpm3.CH0	1		K46
J2.02	no AC	tpm3.CH1	6		R49
J2.86		tpm3.CH2	1		N45
J3.54		tpm3.CH3	4		T48
J3.03		tpm3.EXTCLK	4		M46

8.15.4 TPM4 Signals

Table 81: TPM4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.81		tpm4.CH0	1		L45
J2.14	no AC	tpm4.CH1	6		R51
J2.85		tpm4.CH2	1		N49
J3.64		tpm4.CH3	4		T52
J1.19		tpm4.EXTCLK	4		M48

8.15.5 TPM5 Signals

Table 82: TPM5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.83		tpm5.CH0	1		L49
J2.60		tpm5.CH1	4	Duplicate pin on J3.28	T44
J3.28		tpm5.CH1	4	Duplicate pin on J2.60	T44
J2.08	no AC	tpm5.CH2	6		P52
J2.10	no AC	tpm5.CH3	4		U45
J1.17		tpm5.EXTCLK	4		M52

8.15.6 TPM6 Signals

Table 83: TPM6 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.01		tpm6.CH0	4		M44
J2.54		tpm6.CH1	4	Duplicate pin on J3.36	T46
J3.36		tpm6.CH1	4	Duplicate pin on J2.54	T46
J2.06	no AC	tpm6.CH2	6		R45
J2.60		tpm6.EXTCLK	5	Duplicate pin on J3.28	T44
J3.28		tpm6.EXTCLK	5	Duplicate pin on J2.60	T44

8.16 Low-Power Timer (LPTMR)

The DART-MX95 exports the 2 Low-Power Timer (LPTMR) modules available by the i.MX95 SOC.

You can configure LPTMR to operate as a time counter with an optional prescaler, or as a pulse counter with an optional glitch filter, across all power modes, including low-power modes. It is reset only on Power on Reset (POR) or LowVoltageDetect(LVD), allowing it to be used as a time-of-day counter

The following features characterize Low-Power Timer (LPTMR) Module:

- 32-bit time counter or pulse counter with compare:
  - Optional interrupt that can generate an asynchronous wake-up from any low-power mode
  - Hardware trigger output
  - Counter that supports a free-running mode or reset on compare
- Configurable clock source for prescaler and glitch filter
- Configurable input source for pulse counter (rising-edge or falling-edge)

The AON domain/Wakeup domain support one of the two low power timers on the chip.

8.16.1 LPTMR1 Signals

Table 84: LPTMR1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.50		lptmr1.ALT0	4		F46
J2.56		lptmr1.ALT1	4		G45
J2.48		lptmr1.ALT2	4		H46

8.16.2 LPTMR2 Signals

Table 85: TPM2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.12	no EC	lptmr2.ALT0	3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AK36
J1.84		lptmr2.ALT0	1	Will change level according to J1.90 VDD_SDIO2;	AA49
J1.14	no EC	lptmr2.ALT1	3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AJ37
J1.28		lptmr2.ALT1	1	Recommend using SD2_RESET_B for external SD card power cycle. Will change level according to J1.90 VDD_SDIO2;	AD52
J1.16	no EC	lptmr2.ALT2	3	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); RGMII Data in	AH38

8.17 Flexible I/O (FLEXIO)

The DART-MX95 exports the two FLEXIO interface pins available by the i.MX95 SOC.

FLEXIO is a highly configurable module that provides:

- Emulation of various serial or parallel communication protocols.
- Flexible 16-bit timers with support for various trigger, reset, enable, and disable conditions.
- Programmable logic blocks that allow the implementation of digital logic functions on-chip and configurable interaction of internal and external modules.
- Programmable state machine for offloading basic system control functions from the CPU.

The following features characterize Flexible I/O (FLEXIO) Module:

- Array of 32-bit shift registers with transmit, receive, data match, logic, and state modes:
  - Double-buffered shifter operation for continuous data transfer
  - Shifter concatenation to support large transfer sizes
  - Automatic start and stop bit generation
  - 1, 2, 4, 8, 16, or 32 multi-bit shift widths for parallel interface support
  - Interrupt, DMA, or polled transmit and receive operation
- Highly flexible 16-bit timers with support for various internal or external triggers, reset, enable, and disable conditions:
  - Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during Stop mode
  - Programmable logic mode for integrating external digital logic functions on-chip, or combining pin, shifter, or timer functions to generate complex outputs
  - Programmable state machine for offloading basic system control functions from CPU, with support for up to eight states, eight outputs, and three selectable inputs per state
- Integrated general-purpose I/O registers and pin rising or falling edge interrupts to simplify software support
- Support for a wide range of protocols, including but not limited to:
  - UART
  - I2C
  - SPI
  - I2S
  - Camera IF
  - Motorola 68K or Intel 8080 bus
  - PWM or waveform generation
  - Input-capture (pulse-edge interval measurement), such as SENT

The two FLEXIO instances are in the Wakeup domain.

8.17.1 FLEXIO1 Signals

Table 86: FLEXIO1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.74		flexio1.FLEXIO[0]	4	External SD card detect input; Add 10K external pull up to J1.90; Will change level according to J1.90 VDD_SDIO2;	AD48
J2.20		flexio1.FLEXIO[0]	7	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J49
J1.82		flexio1.FLEXIO[1]	4	Will change level according to J1.90 VDD_SDIO2;	AB48
J2.24		flexio1.FLEXIO[1]	7	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	J51
J1.19		flexio1.FLEXIO[10]	7		M48
J1.17		flexio1.FLEXIO[11]	7		M52
J2.86		flexio1.FLEXIO[12]	3		N45
J2.85		flexio1.FLEXIO[13]	7		N49
J2.89		flexio1.FLEXIO[14]	7		N51
J2.87		flexio1.FLEXIO[15]	7		P44
J2.04	no AC	flexio1.FLEXIO[16]	7		P46
J2.16	no AC	flexio1.FLEXIO[17]	7		P48
J2.08	no AC	flexio1.FLEXIO[18]	7		P52
J2.06	no AC	flexio1.FLEXIO[19]	3		R45
J1.88		flexio1.FLEXIO[2]	4	Will change level according to J1.90 VDD_SDIO2;	AB52
J2.26		flexio1.FLEXIO[2]	7	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K48
J2.02	no AC	flexio1.FLEXIO[20]	7		R49
J2.45	SDEX	flexio1.FLEXIO[20]	4	Available in "SDEX" configuration; Runs @ 1.8V	AG51
J2.14	no AC	flexio1.FLEXIO[21]	3		R51
J2.43	SDEX	flexio1.FLEXIO[21]	4	Available in "SDEX" configuration; Runs @ 1.8V	AF48
J2.35	SDEX	flexio1.FLEXIO[22]	4	Available in "SDEX" configuration; Runs @ 1.8V	AG49
J2.60		flexio1.FLEXIO[22]	7	Duplicate pin on J3.28	T44
J3.28		flexio1.FLEXIO[22]	7	Duplicate pin on J2.60	T44
J2.33	SDEX	flexio1.FLEXIO[23]	4	Available in "SDEX" configuration; Runs @ 1.8V	AH52
J2.54		flexio1.FLEXIO[23]	7	Duplicate pin on J3.36	T46
J3.36		flexio1.FLEXIO[23]	7	Duplicate pin on J2.54	T46
J2.31	SDEX	flexio1.FLEXIO[24]	4	Available in "SDEX" configuration; Runs @ 1.8V	AE49
J3.54		flexio1.FLEXIO[24]	7		T48
J2.29	SDEX	flexio1.FLEXIO[25]	4	Available in "SDEX" configuration; Runs @ 1.8V	AF52
J3.64		flexio1.FLEXIO[25]	7		T52
J2.10	no AC	flexio1.FLEXIO[26]	3		U45
J2.76		flexio1.FLEXIO[26]	4	Runs @ 1.8V	AH20
J2.80		flexio1.FLEXIO[27]	4	Runs @ 1.8V	AF20

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.30		flexio1.FLEXIO[28]	7		U51
J2.32		flexio1.FLEXIO[29]	7		V44
J1.86		flexio1.FLEXIO[3]	4	Will change level according to J1.90 VDD_SDIO2;	AC51
J2.22		flexio1.FLEXIO[3]	7	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage; Always exposed;	K52
J2.01		flexio1.FLEXIO[30]	4	Add external 10K pull down; Runs @ 1.8V	AG21
J3.42		flexio1.FLEXIO[30]	7	Pin has 4.99K pull up on DART	V46
J2.09		flexio1.FLEXIO[31]	4	Runs @ 1.8V	AJ23
J3.46		flexio1.FLEXIO[31]	7	Pin has 4.99K pull up on DART	V48
J1.80		flexio1.FLEXIO[4]	4	Will change level according to J1.90 VDD_SDIO2;	AC49
J2.79		flexio1.FLEXIO[4]	7		K46
J1.78		flexio1.FLEXIO[5]	4	Will change level according to J1.90 VDD_SDIO2;	AA51
J2.81		flexio1.FLEXIO[5]	7		L45
J1.84		flexio1.FLEXIO[6]	4	Will change level according to J1.90 VDD_SDIO2;	AA49
J2.83		flexio1.FLEXIO[6]	7		L49
J1.28		flexio1.FLEXIO[7]	4	Recommend using SD2_RESET_B for external SD card power cycle. Will change level according to J1.90 VDD_SDIO2;	AD52
J2.77		flexio1.FLEXIO[7]	7		L51
J3.01		flexio1.FLEXIO[8]	7		M44
J3.03		flexio1.FLEXIO[9]	7		M46

8.17.2 FLEXIO2 Signals

Table 87: FLEXIO2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.13		flexio2.FLEXIO[0]	4	Runs @ 3.3V level via NTS0104GU12 level translator	AK40
J1.11		flexio2.FLEXIO[1]	4	Runs @ 3.3V level via NTS0104GU12 level translator	AJ39
J1.10	no EC	flexio2.FLEXIO[10]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AJ35
J1.12	no EC	flexio2.FLEXIO[11]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AK36
J1.14	no EC	flexio2.FLEXIO[12]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AJ37
J1.16	no EC	flexio2.FLEXIO[13]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AH38
J2.63		flexio2.FLEXIO[14]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK32
J2.62		flexio2.FLEXIO[15]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ31
J2.73		flexio2.FLEXIO[16]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG29
J2.78		flexio2.FLEXIO[17]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); Internal buffer connected to this pin drives	AF28

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				BOOT_MODE0 (J2.90), latched with POR_B rise. This sets boot source.	
J2.67		flexio2.FLEXIO[18]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG27
J2.70		flexio2.FLEXIO[19]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG25
J1.08	no EC	flexio2.FLEXIO[2]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG37
J2.74		flexio2.FLEXIO[20]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AF24
J2.71		flexio2.FLEXIO[21]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG23
J2.64		flexio2.FLEXIO[22]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AH26
J2.72		flexio2.FLEXIO[23]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ25
J2.65		flexio2.FLEXIO[24]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ27
J2.69		flexio2.FLEXIO[25]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK28
J2.66		flexio2.FLEXIO[26]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ29
J2.68		flexio2.FLEXIO[27]	4	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AH30
J1.06	no EC	flexio2.FLEXIO[3]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AF36
J2.07		flexio2.FLEXIO[30]	4	Runs @ 1.8V	AK24
J2.03		flexio2.FLEXIO[31]	4	Runs @ 1.8V	AH22
J1.02	no EC	flexio2.FLEXIO[4]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG35
J1.04	no EC	flexio2.FLEXIO[5]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG33
J1.03	no EC	flexio2.FLEXIO[6]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AF32
J1.05	no EC	flexio2.FLEXIO[7]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface	AG31
J1.09	no EC	flexio2.FLEXIO[8]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AH34
J1.07	no EC	flexio2.FLEXIO[9]	4	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface	AJ33

8.18 ADC

The DART-MX95 exports the 8 ADC input channels available by the i.MX95 SOC.
The ADC is 12-bit with 1 MS/s. ADC pins are referenced to 1.8V
Refer to i.MX95 Reference manual for more information.
This is available with the special “ADC” assembly configuration.

8.18.1 ADC Signals

Table 88: ADC Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.29	ADC	ADC_IN0		Available in "ADC" configuration; Runs @ 1.8V	A37
J2.15	ADC	ADC_IN1		Available in "ADC" configuration Runs @ 1.8V	B38
J2.17	ADC	ADC_IN2		Available in "ADC" configuration Runs @ 1.8V	C39
J2.58	ADC	ADC_IN3		Available in "ADC" configuration; Runs @ 1.8V	B40
J3.30	ADC	ADC_IN4		Available in "ADC" configuration; Runs @ 1.8V	A41
J3.40	ADC	ADC_IN5		Available in "ADC" configuration; Runs @ 1.8V	B42
J3.60	ADC	ADC_IN6		Available in "ADC" configuration; Runs @ 1.8V	B44
J2.05	ADC	ADC_IN7		Available in "ADC" configuration Runs @ 1.8V	A45

8.19 Reference Clocks

The DART-MX95 exposes the CCM module signals available on normal GPIO pads via IOMUX which can be used to clock external devices.

8.19.1 Clock Signals

Table 89: Clock Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.76		ccmsrcgpcmix.CLKO1	0	Runs @ 1.8V	AH20
J2.80		ccmsrcgpcmix.CLKO2	0	Runs @ 1.8V	AF20
J1.05	no EC	ccmsrcgpcmix.ENET_REF_CLK_ROOT	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface	AG31
J2.71		ccmsrcgpcmix.ENET_REF_CLK_ROOT	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG23
J2.48		ccmsrcgpcmix.EXT_CLK1	6		H46
J1.82		ccmsrcgpcmix.OBSERVE1	6	Will change level according to J1.90 VDD_SDIO2;	AB48
J1.88		ccmsrcgpcmix.OBSERVE2	6	Will change level according to J1.90 VDD_SDIO2;	AB52
J1.86		ccmsrcgpcmix.OBSERVE3	6	Will change level according to J1.90 VDD_SDIO2;	AC51
J1.06	no EC	INPUT=netc.ETH0_RMII_REF50_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT	1	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AF36
J2.78		INPUT=netc.ETH1_RMII_REF50_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT	1	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); Internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise. This sets boot source.	AF28

8.20 GPIO - General Purpose Input Output

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

GPIO_1 is in AON domain, GPIO2-GPIO5 are in Wakeup domain.

8.20.1 GPIO Signals

Table 90: GPIO Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.48		gpio1.IO[10]	5		H46
J2.13		gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]	5	Duplicate pin on J2.42 BOOT_MODE2 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull down; GPIO can be output only or tristated.	G49
J2.42		gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]	5	Duplicate pin on J2.13; see J2.13 note	G49
J2.38		gpio1.IO[12]	5		G51
J1.72		gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]	5	Duplicate pin on J2.44 BOOT_MODE3 pin, Has internal 10K PU to J1.27 (3.3V); Do not drive until after POR_B rise + 30ms; GPIO can be output only or tristated.	H48
J2.44		gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]	5	Duplicate pin on J1.72; see J1.72 note	H48
J2.36		gpio1.IO[14]	5		H52
J2.28		gpio1.IO[15]	5	Recommend using as WDOG_ANY to cold reset the DART with internal watch dog event;	J45
J2.34		gpio1.IO[2]	5		E43
J2.40		gpio1.IO[3]	5		E45
J2.88		gpio1.IO[4]	5	Used as console debug on Variscite release;	E49
J2.90		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]	5	Used as console debug on Variscite release; BOOT_MODE0 pin, Do not drive until after POR_B rise + 30ms; Internal buffer connected to J2.78 drives this pin, latched with POR_B rise; This sets boot source. GPIO can be output only or tristated.	F52
J2.46		gpio1.IO[6]	5		E51
J2.11		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]	5	Duplicate pin on J3.50 (In initial SOM Rev 1.0 on pin J3.48); BOOT_MODE1 pin, Do not drive until after POR_B rise + 30ms;	F48

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				Add 10K pull up to J1.27 (3.3V); GPIO can be output only or tristated.	
J3.50		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]	5	Duplicate pin on J2.11; see J2.11 note (In initial SOM Rev 1.0 exported on pin J3.48)	F48
J2.50		gpio1.IO[8]	5		F46
J2.56		gpio1.IO[9]	5		G45
J2.20		gpio2.IO[0]	0	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage	J49
J2.24		gpio2.IO[1]	0	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage	J51
J1.19		gpio2.IO[10]	0		M48
J1.17		gpio2.IO[11]	0		M52
J2.86		gpio2.IO[12]	0		N45
J2.85		gpio2.IO[13]	0		N49
J2.89		gpio2.IO[14]	0		N51
J2.87		gpio2.IO[15]	0		P44
J2.04	no AC	gpio2.IO[16]	0		P46
J2.16	no AC	gpio2.IO[17]	0		P48
J2.08	no AC	gpio2.IO[18]	0		P52
J2.06	no AC	gpio2.IO[19]	0		R45
J2.26		gpio2.IO[2]	0	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage	K48
J2.02	no AC	gpio2.IO[20]	0		R49
J2.14	no AC	gpio2.IO[21]	0		R51
J2.60		gpio2.IO[22]	0	Duplicate pin on J3.28	T44
J3.28		gpio2.IO[22]	0	Duplicate pin on J2.60	T44
J2.54		gpio2.IO[23]	0	Duplicate pin on J3.36	T46
J3.36		gpio2.IO[23]	0	Duplicate pin on J2.54	T46
J3.54		gpio2.IO[24]	0		T48
J3.64		gpio2.IO[25]	0		T52
J2.10	no AC	gpio2.IO[26]	0		U45
J2.30		gpio2.IO[28]	0		U51
J2.32		gpio2.IO[29]	0		V44
J2.22		gpio2.IO[3]	0	Used on DART for BT communication; If BT not required internal buffer can be disabled and pin function released to customer usage	K52
J3.42		gpio2.IO[30]	0	Pin has 4.99K pull up on DART	V46
J3.46		gpio2.IO[31]	0	Pin has 4.99K pull up on DART	V48
J2.79		gpio2.IO[4]	0		K46

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.81		gpio2.IO[5]	0		L45
J2.83		gpio2.IO[6]	0		L49
J2.77		gpio2.IO[7]	0		L51
J3.01		gpio2.IO[8]	0		M44
J3.03		gpio2.IO[9]	0		M46
J1.74		gpio3.IO[0]	5	External SD card detect input; Add 10K external pull up to J1.90; Will change level according to J1.90 VDD_SDIO2;	AD48
J1.82		gpio3.IO[1]	5	Will change level according to J1.90 VDD_SDIO2;	AB48
J1.88		gpio3.IO[2]	5	Will change level according to J1.90 VDD_SDIO2;	AB52
J2.45	SDEX	gpio3.IO[20]	5	Available in "SDEX" configuration; Runs @ 1.8V	AG51
J2.43	SDEX	gpio3.IO[21]	5	Available in "SDEX" configuration; Runs @ 1.8V	AF48
J2.35	SDEX	gpio3.IO[22]	5	Available in "SDEX" configuration; Runs @ 1.8V	AG49
J2.33	SDEX	gpio3.IO[23]	5	Available in "SDEX" configuration; Runs @ 1.8V	AH52
J2.31	SDEX	gpio3.IO[24]	5	Available in "SDEX" configuration; Runs @ 1.8V	AE49
J2.29	SDEX	gpio3.IO[25]	5	Available in "SDEX" configuration; Runs @ 1.8V	AF52
J2.76		gpio3.IO[26]	5	Runs @ 1.8V	AH20
J2.80		gpio3.IO[27]	5	Runs @ 1.8V	AF20
J2.07		gpio3.IO[28]	5	Runs @ 1.8V	AK24
J2.03		gpio3.IO[29]	5	Runs @ 1.8V	AH22
J1.86		gpio3.IO[3]	5	Will change level according to J1.90 VDD_SDIO2;	AC51
J2.01		gpio3.IO[30]	5	Add external 10K pull down; Runs @ 1.8V	AG21
J2.09		gpio3.IO[31]	5	Runs @ 1.8V	AJ23
J1.80		gpio3.IO[4]	5	Will change level according to J1.90 VDD_SDIO2;	AC49
J1.78		gpio3.IO[5]	5	Will change level according to J1.90 VDD_SDIO2;	AA51
J1.84		gpio3.IO[6]	5	Will change level according to J1.90 VDD_SDIO2;	AA49
J1.28		gpio3.IO[7]	5	Recommend using SD2_RESET_B for external SD card power cycle. Will change level according to J1.90 VDD_SDIO2;	AD52
J1.13		gpio4.IO[0]	5	Runs @ 3.3V level via NTS0104GU12 level translator	AK40
J1.11		gpio4.IO[1]	5	Runs @ 3.3V level via NTS0104GU12 level translator	AJ39
J1.10	no EC	gpio4.IO[10]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AJ35
J1.12	no EC	gpio4.IO[11]	5	Available in "no EC" configuration;	AK36

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				IO level follows J1.31 (1.8V/3.3V)	
J1.14	no EC	gpio4.IO[12]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AJ37
J1.16	no EC	gpio4.IO[13]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AH38
J2.63		gpio4.IO[14]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK32
J2.62		gpio4.IO[15]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ31
J2.73		gpio4.IO[16]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG29
J2.78		gpio4.IO[17]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V); Internal buffer connected to this pin drives BOOT_MODE0 (J2.90), latched with POR_B rise. This sets boot source.	AF28
J2.67		gpio4.IO[18]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG27
J2.70		gpio4.IO[19]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG25
J1.08	no EC	gpio4.IO[2]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG37
J2.74		gpio4.IO[20]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AF24
J2.71		gpio4.IO[21]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AG23
J2.64		gpio4.IO[22]	5	In "EC" configuration- Runs@1.8V;	AH26

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	
J2.72		gpio4.IO[23]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ25
J2.65		gpio4.IO[24]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ27
J2.69		gpio4.IO[25]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AK28
J2.66		gpio4.IO[26]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AJ29
J2.68		gpio4.IO[27]	5	In "EC" configuration- Runs@1.8V; In "no EC" configuration- IO level follows J1.31 (1.8V/3.3V)	AH30
J1.06	no EC	gpio4.IO[3]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AF36
J1.02	no EC	gpio4.IO[4]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG35
J1.04	no EC	gpio4.IO[5]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AG33
J1.03	no EC	gpio4.IO[6]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AF32
J1.05	no EC	gpio4.IO[7]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI filter having ~2ns delay; required for EMI and delay for RGMII interface	AG31
J1.09	no EC	gpio4.IO[8]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V)	AH34
J1.07	no EC	gpio4.IO[9]	5	Available in "no EC" configuration; IO level follows J1.31 (1.8V/3.3V); SOC pin output via EMI	AJ33

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
				filter having ~2ns delay; required for EMI and delay for RGMII interface	
J1.48		gpio5.IO[0]	5	Runs @ 1.8V	AJ45
J1.32		gpio5.IO[1]	5	Runs @ 1.8V	AH46
J1.34		gpio5.IO[10]	5	Runs @ 1.8V	AJ41
J1.47		gpio5.IO[11]	5	Runs @ 1.8V	AH42
J3.38		gpio5.IO[12]	0		V52
J3.48		gpio5.IO[13]	0	(In initial SOM Rev 1.0 exported on pin J3.50)	W45
J3.52		gpio5.IO[14]	0		W49
J3.58		gpio5.IO[15]	0		W51
J3.62		gpio5.IO[17]	0		Y52
J1.50		gpio5.IO[2]	5	Runs @ 1.8V	AJ47
J1.46		gpio5.IO[3]	5	Runs @ 1.8V	AK48
J2.55		gpio5.IO[4]	5	Runs @ 1.8V	AJ49
J2.57		gpio5.IO[5]	5	Runs @ 1.8V	AK50
J2.59		gpio5.IO[6]	5	Runs @ 1.8V	AJ51
J2.61		gpio5.IO[7]	5	Runs @ 1.8V	AH50
J1.38		gpio5.IO[8]	5	Runs @ 1.8V	AK44
J1.40		gpio5.IO[9]	5	Runs @ 1.8V	AJ43

8.21 DAP - Debug Access Port

DAP is a standard Arm component, comprising of several components. These components are used to access the DAP from an external debugger and Access Ports to access on-chip debug system resources. The DAP supports 1149.1/Arm SW-DP interface, which means that the JTAG interface can be operated in either standard 5-pin JTAG-DP interface or in 2-pin SW-DP interface.

The DART-MX95 exposes DAP interface signals.

8.21.1 DAP signals

Table 91: DAP Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.01		dap.TCLK_SWCLK	0	Add external 10K pull down; Runs @ 1.8V	AG21
J3.64		dap.TCLK_SWCLK	5		T52
J2.07		dap.TDI	0	Runs @ 1.8V	AK24
J2.10	no AC	dap.TDI	5		U45
J2.09		dap.TDO_TRACESWO	0	Runs @ 1.8V	AJ23
J3.54		dap.TDO_TRACESWO	5		T48
J2.03		dap.TMS_SWDIO	0	Runs @ 1.8V	AH22

8.22 Power

8.22.1 Power

Table 92: Power Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.15		VDD_BBSM_1V8		BBSM domain power output 1.8V	PF09.16
J1.27		VDD_3V3		Power output from PMIC; Powers all 3.3V Ios; Recommend to use as base board 3.3V regulator enable;	PF09.49
J1.31		ETH_3V3		PF09 PMIC LDO1 output; In "EC" configuration - Ethernet PHY 3.3V power supply In "no EC" configuration - NVCC_ENET domain power supply setting ENET1/2 reference voltage: Default - 3.3V, should be set to 1.8V for ENET1/2 RGMII support Max. 200mA draw allowed;	PF09.53
J1.90		VDD_SDIO2		Power output for SD2 pins reference 1.8V/3.3V- set by DART PMIC;	PF09.3
J2.41		VDD_1V8		1.8V Power output from PMIC; Powers all 1.8V Ios	PF09.21
J3.15	no CMP	VBAT		In CMP configuration this pin is not connected,	VBAT
J3.27	no CMP	VBAT		In CMP configuration this pin is not connected,	VBAT
J3.34	no CMP	VBAT		In CMP configuration this pin is not connected,	VBAT
J3.63	no CMP	VBAT		In CMP configuration this pin is not connected,	VBAT
J3.71		VBAT			VBAT
J3.73		VBAT			VBAT
J3.75		VBAT			VBAT
J3.77		VBAT			VBAT
J3.79		VBAT			VBAT
J3.81		VBAT			VBAT
J3.83		VBAT			VBAT
J3.85		VBAT			VBAT
J3.87		VBAT			VBAT
J3.89		VBAT			VBAT

8.22.2 Ground

Table 93: Ground Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.12		AGND		Connect to GND;	AGND
J1.18		GND			GND
J1.21		GND			GND
J1.30		GND			GND
J1.33		GND			GND
J1.49		GND			GND
J1.52	no BTRST	GND			GND
J1.55	no WBE	GND			GND
J1.58	no WRST	GND			GND
J1.61	no WBE	GND			GND
J1.64	no RFCTRL	GND			GND
J1.67	no WBE	GND			GND
J1.70	no BTRST	GND			GND
J1.76		GND			GND
J1.85		GND			GND
J2.18		GND			GND
J2.23		GND			GND
J2.47		GND			GND
J2.53		GND			GND
J2.75		GND			GND
J2.84		GND			GND
J3.09		GND			GND
J3.10		GND			GND
J3.21		GND			GND
J3.24		GND			GND
J3.33		GND			GND
J3.39		GND			GND
J3.45		GND			GND
J3.51		GND			GND
J3.57		GND			GND
J3.68		GND			GND
J3.74		GND			GND

8.22.3 Not Connected Pins

Table 94: NC Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.03		NC		In "EC" configuration this pin is Not Connected.	NC
J1.23	no WBD/WBE	NC		in "no WBD" or "no WBE" configuration this pin is Not Connected.	NC
J1.25	no WBD/WBE	NC		in "no WBD" or "no WBE" configuration this pin is Not Connected.	NC
J1.29	no ADC	NC			NC
J1.36	no BTPCM	NC			NC
J1.39	no RFCTRL	NC			NC
J1.41	no WBE	NC			NC
J2.05	no ADC	NC			NC
J2.15	no ADC	NC			NC
J2.17	no ADC	NC			NC
J2.19		NC			NC
J2.21		NC			NC
J2.29	no SDEX	NC			NC
J2.31	no SDEX	NC			NC
J2.33	no SDEX	NC			NC
J2.35	no SDEX	NC			NC
J2.37	no COEX	NC			NC
J2.39	no COEX	NC			NC
J2.43	no SDEX	NC			NC
J2.45	no SDEX	NC			NC
J2.52	no WBD/WBE	NC		in "no WBD" or "no WBE" configuration this pin is Not Connected.	NC
J2.58	no ADC	NC			NC
J2.82	no EC	NC			NC
J3.15	CMP	NC			NC
J3.27	CMP	NC			NC
J3.30	no ADC	NC			NC
J3.32	no WBE	NC			NC
J3.34	CMP	NC			NC
J3.40	no ADC	NC			NC
J3.60	no ADC	NC			NC
J3.63	CMP	NC			NC
J3.69		NC			NC
J3.70	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC
J3.72	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC
J3.76	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC
J3.78	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC
J3.80	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.82	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC
J3.84	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC
J3.86	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC
J3.88	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC
J3.90	DSCM	NC		In "DSCM "(DSI Compatible mode) configuration pin is not connected, Instead, MIPI DSI will appear on same pins as DT8M & DT8MM	NC

8.23 System Control

8.23.1 System Control Signals

The user must ensure not to drive any pins/function of the SOM before the appropriate IO domain power is up.

VDD_3V3 output is used to power most of the SOM pins and could be used to control the custom board power. Refer to VAR-DT8MCustomBoard schematics for implementation suggestion.

Table 95: System Control Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.01		PF09_INT_B_ PF53_SOC_PG_ PF53_ARM_PG		PF09 interrupt, PF5302 PGOOD, PF5301 PGOOD signals AND connected with internal PU (In initial SOM Rev 1.0 PF09 interrupt not connected)	
J1.20		bbsmmix.ONOFF	0	SOC input with internal 100K PU; Runs @ VDD_BBSM_1V8 level; In OFF mode: brief connection to GND causes the internal power management state machine to change state to ON. In ON mode: brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). To Force OFF: approximate 5 second or more connection to GND If not used leave Floating;	F40
J1.22		PWRON		SoC output with 100K PD connected to PF09 PMIC PWRON input; Pull low to hold DART internal regulators OFF; Pulse low for cold reboot; Runs @ VDD_BBSM_1V8 level	PF09.28
J1.26		ccmsrcgpcmix.PMIC_STBY_REQ	0	SOC output with 100K PD connected to PF09 PMIC STBY input; Can be used externally to control carrier board power for standby state; Active-high output for going to SUSPEND state; Runs @ VDD_BBSM_1V8 level	C43
J1.24		bbsmmix.POR_B	0	PMIC output with 100K PU connected to SOC; Can be pulled low externally to cause warm reset. Runs @ VDD_BBSM_1V8 level;	D42
J2.49		bbsmmix.TAMPER0	0	Runs @ VDD_BBSM_1V8 level	F36
J2.51		bbsmmix.TAMPER1	0	Runs @ VDD_BBSM_1V8 level	D38
J2.28		wdog1.WDOG_ANY	0	Recommend using as WDOG_ANY to cold reset the DART with internal watch dog event;	J45

8.23.2 Boot configuration

The DART-MX95 can be boot from the following sources:

- Internal source -
  - eMMC Flash memory
- External source -
  - SD Card
  - USB UUU Serial Downloader (BOOT_MODE pins set to boot from SD Card and SD card is not plugged in)

The BOOT_MODE pins determine the boot source.

NOTE

For compatibility with DART-MX8M and DART-MX8M-MINI pin J2.78 which is SAI1_TXD2 (BOOT_CONFIG [10]) in those SOMs, is connected internally via buffer to BOOT_MODE0 of DART-MX95 as boot source selection.

8.23.2.1 Boot Configuration Signals

Table 96: BOOT_MODE Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.13		gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]	5	Duplicate pin on J2.42 BOOT_MODE2 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull down; GPIO can be output only or tristated.	G49
J2.42		gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]	5	Duplicate pin on J2.13; see J2.13 note	G49
J1.72		gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]	5	Duplicate pin on J2.44 BOOT_MODE3 pin, Has internal 10K PU to J1.27 (3.3V); Do not drive until after POR_B rise + 30ms; GPIO can be output only or tristated.	H48
J2.44		gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]	5	Duplicate pin on J1.72; see J1.72 note	H48
J2.90		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]	5	Used as console debug on Variscite release; BOOT_MODE0 pin, Do not drive until after POR_B rise + 30ms; Internal buffer connected to J2.78 drives this pin, latched with POR_B rise; This sets boot source. GPIO can be output only or tristated.	F52
J2.11		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]	5	Duplicate pin on J3.50 (In initial SOM Rev 1.0 on pin J3.48); BOOT_MODE1 pin, Do not drive until after POR_B rise + 30ms; Add 10K pull up to J1.27 (3.3V); GPIO can be output only or tristated.	F48
J3.50		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]	5	Duplicate pin on J2.11; see J2.11 note (In initial SOM Rev 1.0 exported on pin J3.48)	F48

Table 97: Available boot sources

BOOT_MODE	BOOT_CORE	BOOT DEVICE	NOTES
0000	Cortex-A55	From internal fuses	
0001	Cortex-A55	USB1/2 Serial Downloader (USB1 by default; if need to support USB2, should program a fuse.)	
0010	Cortex-A55	USDHC1 8-bit eMMC 5.1	
0011	Cortex-A55	USDHC2 4-bit SD 3.0	
0100	Cortex-A55	FlexSPI Serial NOR with SFDP (JESD-216) discoverable parameters	
0101	Cortex-A55	FlexSPI Serial NAND 2K page	
0110	Cortex-A55	Reserved	
0111	Cortex-A55	Reserved	
1000	Cortex-M33	From internal fuses	
1001	Cortex-M33	USB1/2 Serial Downloader (USB1 by default; if need to support USB2, should program a fuse.)	Variscite EVK and SW support this mode
1010	Cortex-M33	USDHC1 8-bit eMMC 5.1	Variscite EVK and SW support this mode
1011	Cortex-M33	USDHC2 4-bit SD 3.0	Variscite EVK and SW support this mode
1100	Cortex-M33	FlexSPI Serial NOR with SFDP (JESD-216) discoverable parameters	
1101	Cortex-M33	FlexSPI Serial NAND 2K page	
1110	Cortex-M33	Reserved	
1111	Cortex-M33	Reserved	

9. Electrical specifications

9.1 Absolute maximum ratings

Table 98: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBAT	-0.3	6	V
USB_VBUS	-0.3	5.25	V

9.2 Operating conditions

Table 99: Operating Ranges

Parameter	Min.	Typ.	Max.	Unit
VBAT	3.5	3.7	5	V
USB_VBUS	4.75	5	5.25	V

9.3 Power consumption

Table 100: DART-MX95 Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.84V	1015mA	3.89W	Linux up, Wi-Fi connected and Iperf is running 802.11ax 5GHz
Run	3.84V	910mA	3.49W	Linux up, Wi-Fi connected and Iperf is running 802.11n 2.4GHz
Run	3.84V	922mA	3.54W	Linux up. Ethernet0 running Iperf
Run	3.84V	770mA	2.95W	Linux up.
FHD video playback	3.84V	855mA	3.28W	On 800x400 LCD
Suspend	3.84V	TBD	TBD	Memory in retention mode
Off (RTC)	3.84V	TBD	TBD	All power rails are Off, only Internal SoC RTC is powered

NOTE

Setup:
HW: VSM-DT95-003 (DART-MX95H_1800C_8R_32G_AC_EC_WBD_ET_REV1.0)
SW: mx95-yocto-nanbield-6.6.3_1.0.0-v1.0

DISCLAIMER:

Power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.

Depending on the specific use cases and end product system design, an appropriate thermal solution should be applied.

9.4 Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or output to the DART-MX95 uses 3.3V LVCMOS levels, except the following:

SD, ENET, XSPI, PCIe, USB, ETH, MIPI-DSI, MIPI-CSI, LVDS, TAMPER, ADC, WBD/WBE, JTAG, CODEC.

***PCIe, USB, ETH, MIPI-DSI, MIPI-CSI, LVDS*:** Interfaces follow a different standard since they are high-speed signals.

SD2: interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities.

SD3: interface is available in case SOM is ordered **with "SDEX"** configuration, IOs will run at 1.8V.

ENET:
In "EC" configuration - IOs will run at 1.8V
In "no EC" configuration - IO level follows J1.31 (1.8V/3.3V): Default - 3.3V, should be set to 1.8V for ENET1/2 RGMII support.

XPSI/TAMPER/ADC/JTAG: IOs will run at 1.8V.

WBD/WBE: signals which are always exported from WIFI, or signals exported from WIFI in case of one of the special assembly options: BTPCM, SPICM, COEX, BTRST, WRST, RFCNTL.

CODEC: DMIC interface available with “AC” configuration is a mixed voltage; DMIC_CLK outputs at 3.3V levels, but the DMIC_DATA input tolerates 1.8V levels only.

10. Environmental Specifications

Table 101: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> 5737 Khrs	

NOTE

Extended and industrial temperature ranges based only on the operating temperature grade of the SOM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

11. Mechanical Drawings

11.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

NOTE

The size and footprint of SOM 90-pin connectors Hirose P/N: DF40C-90DP-0.4V(51) are different from mating carrier board 90-pin connectors (see section 7.1).

To ensure correct positioning of the carrier board connectors and holes please refer to VAR-DT8MCustomBoard DXF available here (under documentation tab):
http://www.variscite.com/products/single-board-computers/var-dt8mcustomboard

It is recommended NOT to place any components under the SOM.

11.2 Standoffs

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

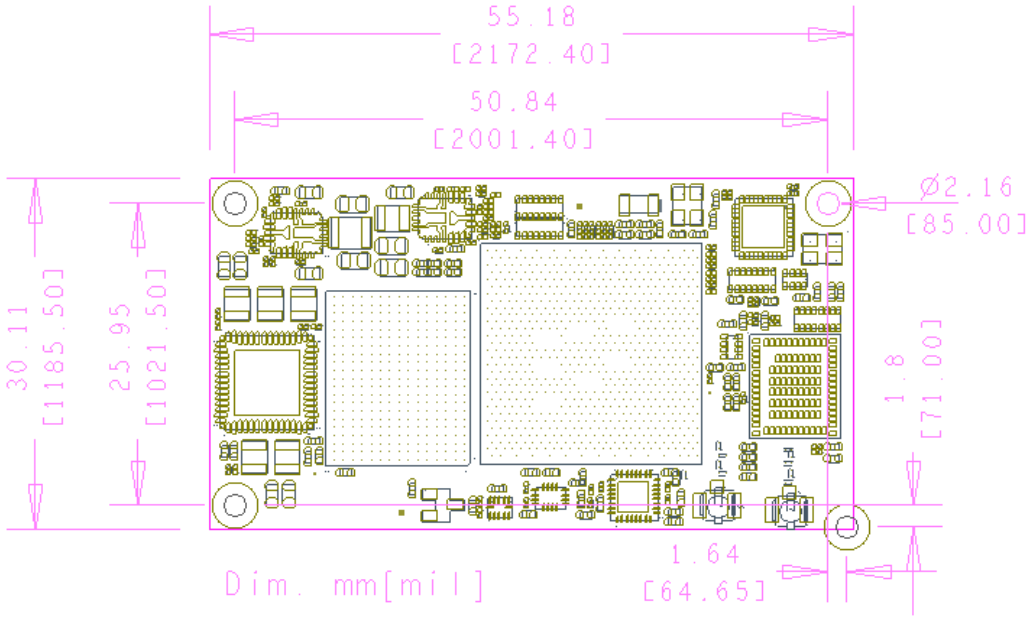
Manufacturer: **MAC8**

PN: **TH-1.6-1.5-M2**

Link: https://www.mac8japan.com/products/258

11.3 SOM Dimensions

Figure 5 illustrates the top view of the DART-MX95 size and mounting holes relative location. **All dimensions given in millimeter and [mils] units**.



UNITS: Milimeters

Figure 5: DART-MX95 Top View Mechanics

11.3.1 CAD Files

CAD files are available for download at http://www.variscite.com/

12. Legal Notice

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Testing and other quality control techniques are utilized to the extent that Variscite deems necessary to support its warranty.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

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